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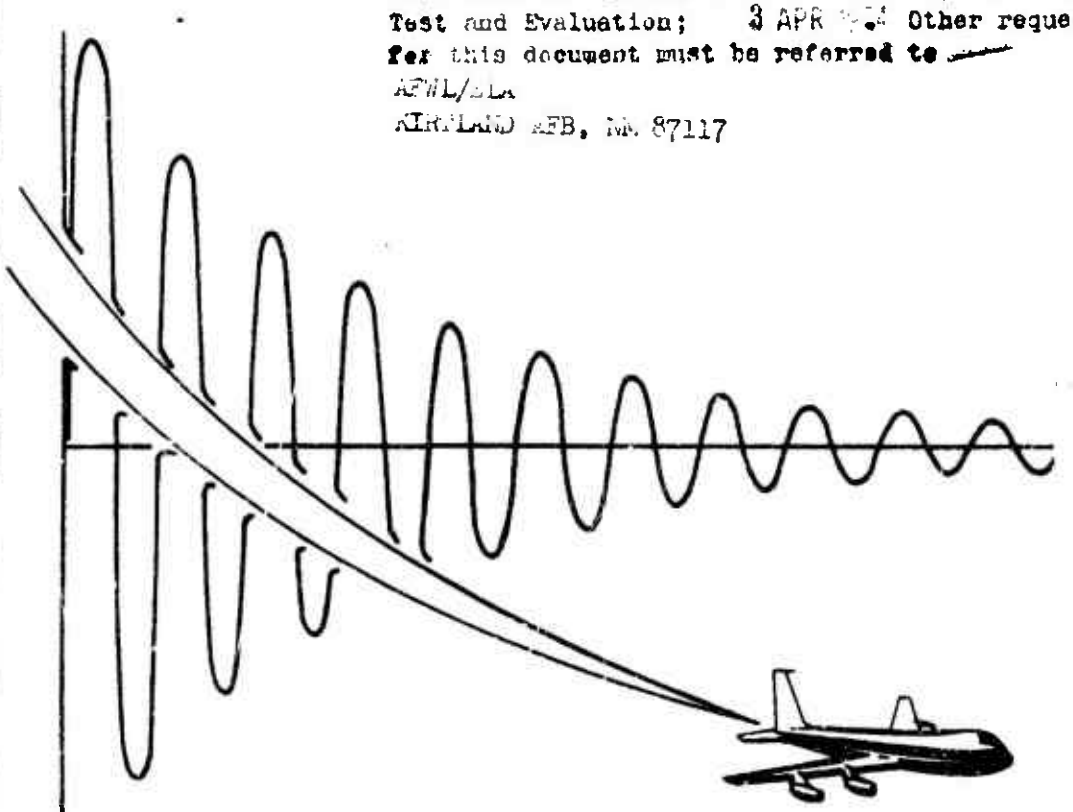
EMP

ELECTRONIC ANALYSIS HANDBOOK

MAY 1973



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ELECTRONIC ANALYSIS

HANDBOOK

MAY 1973

PREPARED UNDER CONTRACT NO. F29601-72-C-0028
PROJECT OFFICER CAPT. G. MICHAELIDIS

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BY

THE BOEING COMPANY
SEATTLE, WASHINGTON

AND

BRADDOCK, DUNN AND McDONALD, INC.
ALBUQUERQUE, NEW MEXICO

FOR

U.S. AIR FORCE WEAPONS LABORATORY
KIRTLAND AIR FORCE BASE
ALBUQUERQUE, NEW MEXICO

PREFACE

The goal in preparing this handbook for EMP Electronic Analysis was to provide the circuit designer with techniques and models for use in aaseaaing the degree of hardness of the circuits he is designing. New concepts and interpretation of existing techniques are presented and will serve as a basis for defining the future effort required to provide a complete subsystem analysis capability.

Section I gives a brief overview of the vsrious facets of a Susceptibility Threshold Analysis. Section II discuases upset threshold analysis including response considerations, selection of analysis method, data, and examples. Section III analyzes the problem of circuit damage thresholds encompassing the same areas as Section II. Section IV describes and illustrates methods for determining cable source characteristics. The handbook also includes several appendices which present some analysis details, a semiconductor damage data base and a discussion of the Driving Point Impedance (DPI) analysis method.

The handbook was prepared by Aeronautical Systems EMP program personnel of the Aerospace Group, The Boeing Company, P.O. Box 3999, Seattle, Washington 98124, and their subcontractor Braddock, Dunn and McDonald, Inc., First National Bank Building East, Albuquerque, New Mexico 87108.

The Program Manager is J. J. Dicomes and the Technical Director is W. L. Gurtis. The principal investigator for this work order is B. P. Gage. BDM efforts on this program are directed by J. J. Schwarz. Contributors to this volume are D. Durgin, B. Gage, C. Jenkina, R. Kelly, W. Pesch, G. Rimbert, J. Schwarz, and M. L. Vincent. The technical editora are B. Gage and D. Durgin.

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SECTION I

INTRODUCTION

1. BACKGROUND

Modern strategic and command aircraft are required to survive the effects of nuclear detonations such that mission objectives are fulfilled. These effects include overpressure, thermal and X-ray fluence, particulate bombardment (neutrons, gamma, etc.), ionizing radiation, and the nuclear electromagnetic pulse (EMP).

EMP is an important adverse environment for two major reasons. First, from an operational point of view, high-intensity electromagnetic fields may exist at very long ranges from the burst location. Considering anti-ballistic missile (ABM) deployment, high-intensity EMP may be expected throughout most of the timeline for typical strategic aircraft missions. This is in contrast to the other nuclear environments which diminish in intensity rapidly with respect to distance from the burst. The other significant feature of EMP is its complex interaction, first with the airframe and subsequently with the internal electronic subsystems. Briefly stated, the airframe acts as a large antenna in responding to the field of the EMP. Skin currents and charges are generated which in turn cause internal fields through apertures, gaps, discontinuities, and by pickup on exposed cables. These internal fields induce voltage transients into interconnecting cabling which in turn gives rise to currents which affect the electronic equipment. Since the phenomenological and coupling aspects of nuclear EMP generation, propagation, and interaction are described in considerable detail in numerous published sources (References 1-3), it is sufficient to say here that EMP can cause large voltage and current transients that result in anomalous responses in electronic systems.

The determination of the smallest EMP induced signal amplitude of a given time history, that will produce a subsystem malfunction, is called an EMP Susceptibility Threshold Analysis. EMP related subsystem malfunctions are broadly divided into two categories, namely upset and damage.

The minimum signal level that will cause a permanent degradation in subsystem performance is defined as the Damage Threshold. Damage is basically a component level response in that the subsystem performance degradation can be directly related to the failure of one or more electronic parts.

The minimum signal level that can csuse a transient or nonpermanent degradation of a subsystem's functionsl capabilities is defined as the Upset Threshold. Upset is basically a circuit and subsystem level response in that a spurious circuit operation must occur and must produce an unacceptable subsystem response before upset can be said to have occurred.

The results of an EMP Susceptibility Threshold Analysis combined with the results of an EMP Coupling Anslysis are used to perform s Vulnerability Assessment of a given subsystem. The objective of s gensrsl threshold analysis is to compute circuit upset or damage threshold independent of any specific driving function or source impedsnce. In actuslity, the subsystem analyst has been given an EMP specification and the performance of a circuit threshold analysis and a vulnerability sssessment are inseparable. Therefore, this handbook provides guidelines for performing both EMP Susceptibility Threshold Analysis and circuit level Vulnersbility Assessment. It should be noted that a specific driving function and a source impedance are not required to perform a threshold analysis. In this case, either the threshold voltage, current, or power is determined at the subsystem interface and csn be used to compute generator voltage for any given source impedance.

The hardening of a subsystem refers to the reduction of its vulnerability by either increasing its susceptibility thresholds or by reducing its exposure to coupled energy or possibly both. Subsystem hardening is discussed in detail in Reference 4.

2. SCOPE

The purpose of this handbook is to present general methodologies for, and specific examples of, the computation of damage and upset thresholds for typical electronic circuits. The methods presented use conventional circuit analysis techniques in combination with unique component and circuit response modeling methods to achieve the prediction of upset and damage signal levels.

Since electronic design engineers routinely use conventional circuit analysis methods such as Kirchoff's Laws, network theorems (superposition, Norton's and Thevenin's), breakpoint analysis and Driving Point Impedance (DPI) techniques, this handbook does not include a tutorial coverage of this material. The emphasis is placed on presenting available information regarding the abnormal circuit and device response characteristics associated with the large amplitude, high frequency transients associated with EMP.

One section of this handbook is devoted to the description and application of a typical EMP subsystem specification. Methods for computing interface signals and related source impedances are presented. This information in combination with the threshold analysis techniques presented can be used to determine circuit vulnerability.

3. SUSCEPTIBILITY ANALYSIS OVERVIEW

a. General

The analysis of an electronic system's susceptibility to some mode of malfunction as a direct result of an EMP induced transient,

requires the estimation or computation of the upset and/or damage threshold of each circuit found to have a significant effect on the system's performance. The identification of relevant circuits involves a detailed review of all circuits and the rejection of unimportant ones based on either the presence of acceptsble protection or functional irrelevance. This screening procedure is quite straightforward although very time consuming and is summarized in Figure I-1. This procedure is applicable to any subsystem that must meet an EMP specification or, in the absence of such a specification, to any subsystem deemed critical to the successful completion of a system's mission in a nuclear environment.

As part of evaluating the upset and damage thresholds of a subsystem, the analyst must become intimately familiar with its detailed configuration and operation. The use of this information differs for the upset and damage cases and is discussed in more detail below.

b. Damage Considerations

Damage has been defined ss an irreversible degradation of component functional capsbilities. In theory, any electronic component is potentially susceptible to EMP caused damage. In fact, some component types are inherently hard to the levels of EMP transients likely to be experienced in aeronautical systems and some damageable components are protected by buffering networks made up of less sensitive components (e.g., series resistor or inductors, and shunt capacitors). Therefore, if a worst case transient amplitude and frequency distribution can be either estimated or legislated before initiating the damage threshold analysis, circuit rejection criteria can be established that will reduce the number of circuits which must be analyzed in detail.

If a system EMP specification has been defined (such ss Figure I-2 which applies to the B-1 aircraft) then the worst case can be determined and the circuit sorting can proceed using a "quick look" circuit analysis

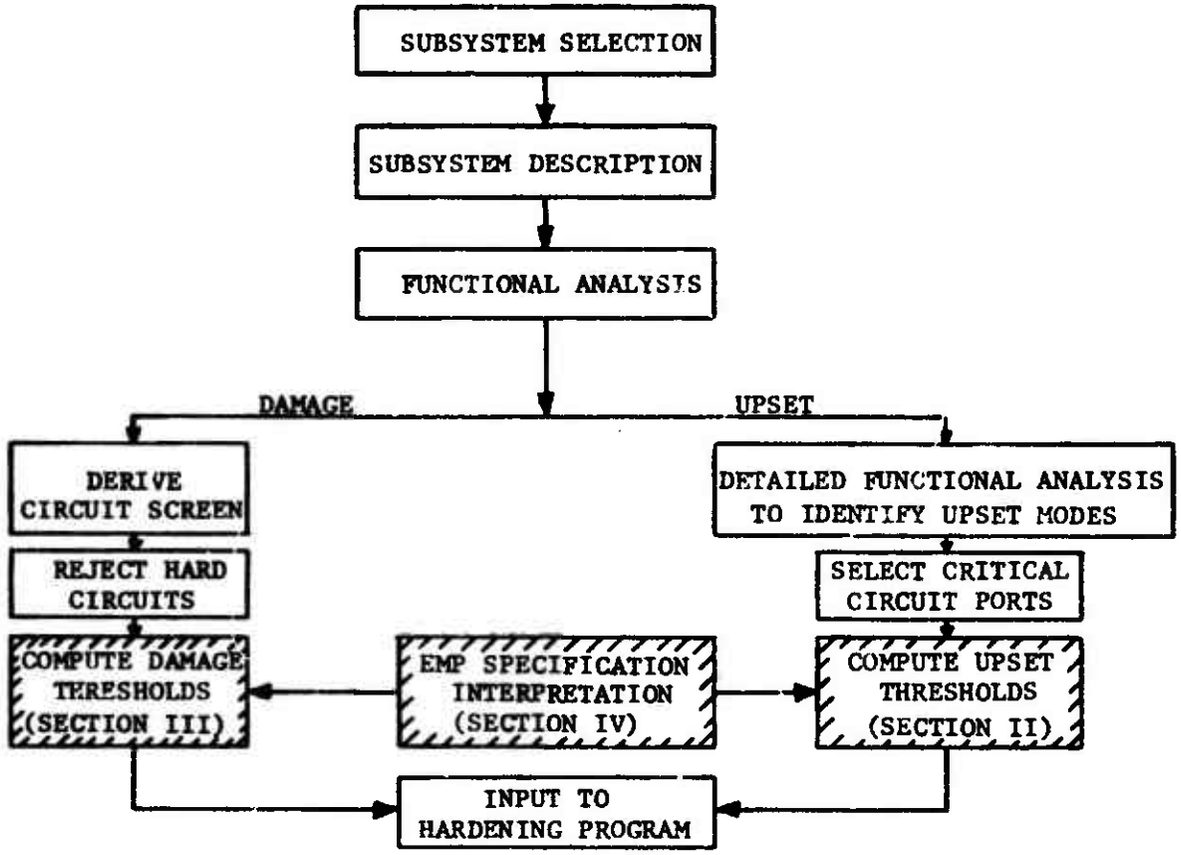
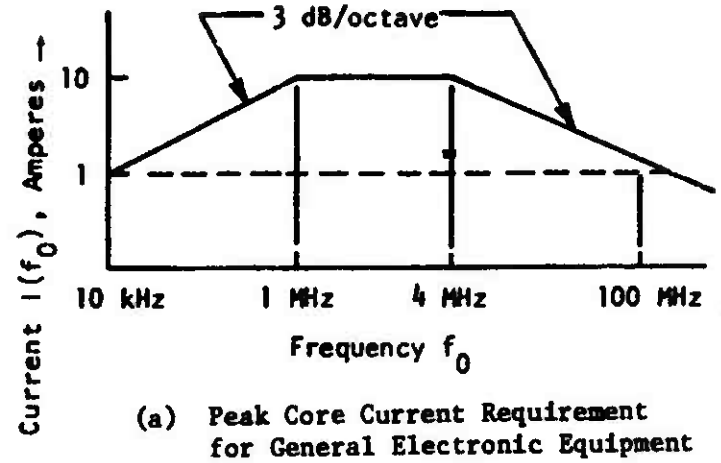
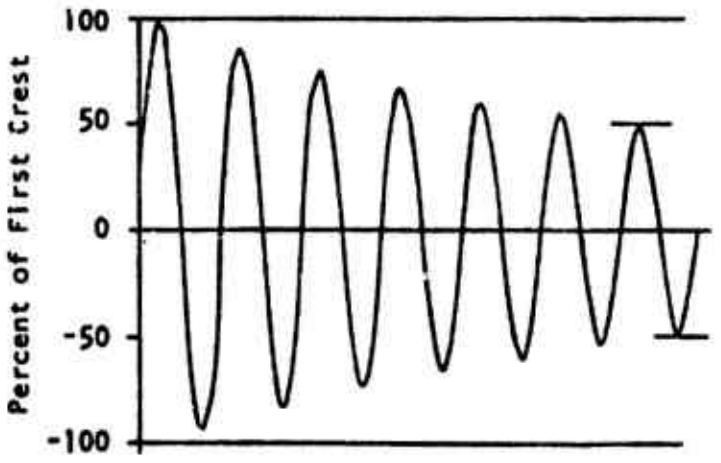


Figure I-1. Screening Procedure Summary



(a) Peak Core Current Requirement for General Electronic Equipment



(b) Cable Core Current Waveshape

Figure I-2. EMP Interference Test Specifications for B-1 Mission Critical Avionics

procedure. Such a procedure is discussed in detail in References 5 and 6 and consists basically of defining circuit configurations that are not damageable at specified worst case transient levels.

If an EMP specification has not been defined for a given subsystem, then a worst case specification can be estimated based on known physical constraints such as cable or connector voltage breakdown and system or subsystem geometry. Depending on the location of the subsystem and its associated cabling, the range of worat case EMP signals is typically from 1 to 1000 amperes for a maximum voltage of perhaps 10 kV and pulse durations of less than 100 microseconds. Some rare circuits connected to efficient antennas may experience higher levels, but the given range can be considered an extreme worst case in most instances. The selection of a specific worst case specification in the range given necessitates considerable familiarity with the subsystem being analyzed.

As shown in Figure I-1, circuits that survive the screening procedure are then analyzed in detail to determine their damage thresholds. Section III presents detailed methods and examples illustrating the computation of circuit damage thresholds.

c. Upset Considerations

Upset may be defined as a nonpermanent anomalous response which results in the degradation of system functional capabilities. Thus, an EMP event may cause a variety of transient responses in various subaystems and circuits, but unless a degradation of aystem capability results, there is no upset. Given this definition, it can be seen that an individual upset is not uniquely defined. Whether or not an EMP-induced signal produces an upset depends on both electrical parameters such as amplitude and duration, and operational parameters such as circuit or subsystem criticality and mission description.

As shown in Figure I-1, the determination of upset thresholds requires first that the analyst be intimately familiar with the subsystem operation, and second, that he select circuits that, when perturbed, cause the subsystem to malfunction. Given a specific circuit, Section II presents detailed methods and examples illustrating circuit upset threshold computation.

From the above discussion, it may be surmised that the definition of upset is concise and technically correct, but perhaps not particularly helpful in gaining an understanding of upset phenomena. This is a consistent problem in discussing upset. Any attempt to provide general guidelines requires so many qualifications that the complexity precludes understanding. The following discussion is intended to clarify the concept of transient upset.

System upset can result from either the generation of erroneous data or the loss of valid data. In general, upset may result from the anomalous response of either analog or digital circuitry. However, in many cases the determination of whether an anomalous response actually constitutes an upset will depend on its timing relative to other system parameters (e.g., Is a clock pulse present? Are the data critical during this portion of the mission?). In these cases, the probability of upset increases with the duration of the anomalous response. Thus, the probability of upset increases as a circuit's ability to "remember" transients increases. Digital circuitry inherently provides a greater memory capability than analog circuitry. Thus, digital circuitry receives more emphasis in discussions of upset. However, in certain cases, especially if latch-up or saturation occurs, analog circuits can exhibit a memory of considerable duration. At any rate, it should be recalled that memory is not always necessary to produce upset, it merely increases the probability. Figure I-3 presents three examples of anomalous circuit responses that

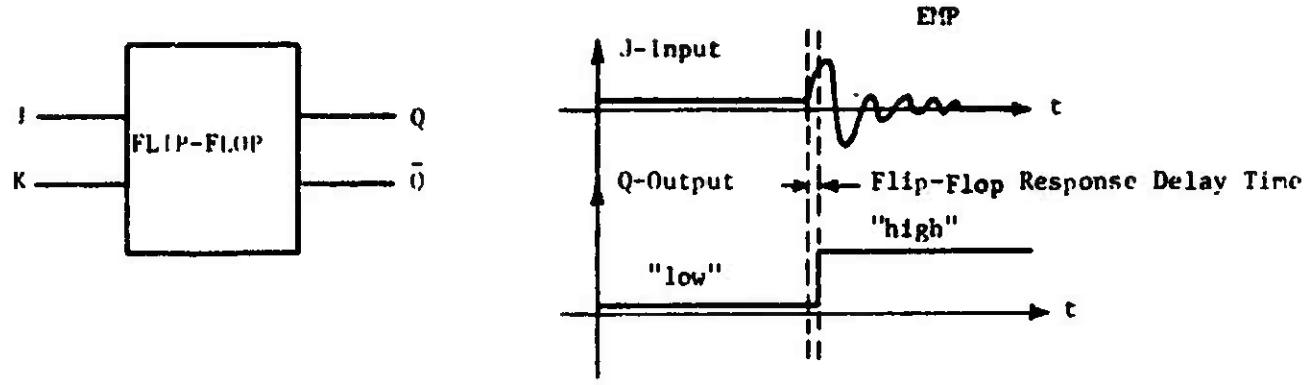
could produce upset, given an appropriate operational situation. These examplea are provided to gain a practical insight into upset mechanisms.

Figure I-3a illustrates a flip-flop circuit which changea state due to an EMP transient on a trigger input. This is perhapa the classical upaet example. Erroneous data have been generated. Unlesa the flip-flop is reset, it will remain in the changed state permanently. If the data which the flip-flop state represents are critical, the system functional capability will be degraded and upset will have occurred. On the other hand, if the flip-flop is reaet before the data are needed (i.e., become critical), the system will not be degraded and upset has not occurred.

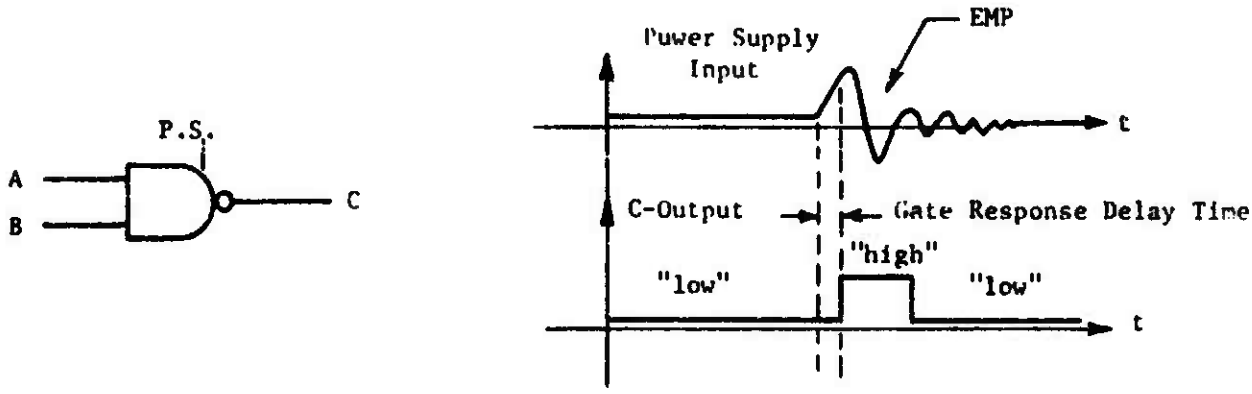
Figure I-3b shows a NAND gate changing its output logic level temporarily due to an EMP transient on the power supply input. If the system is configured to recognize this temporary logic shift as data, then upaet may occur. If the system doea not recognize the logic shift as data (e.g., if the system responds too slowly), then upset does not occur.

Figure I-3c shows an amplifier being driven into saturation by an EMP transient superimposed on its signal input. Here, the data channel is interrupted and all valid data are lost as long as the amplifier remains in saturation. If critical data are lost, then the system capability is degraded and upset has occurred. If no data were present, or if the outage time was insufficient to destroy any data, or if the data were not critical; then no degradation, and thus no upset has occurred.

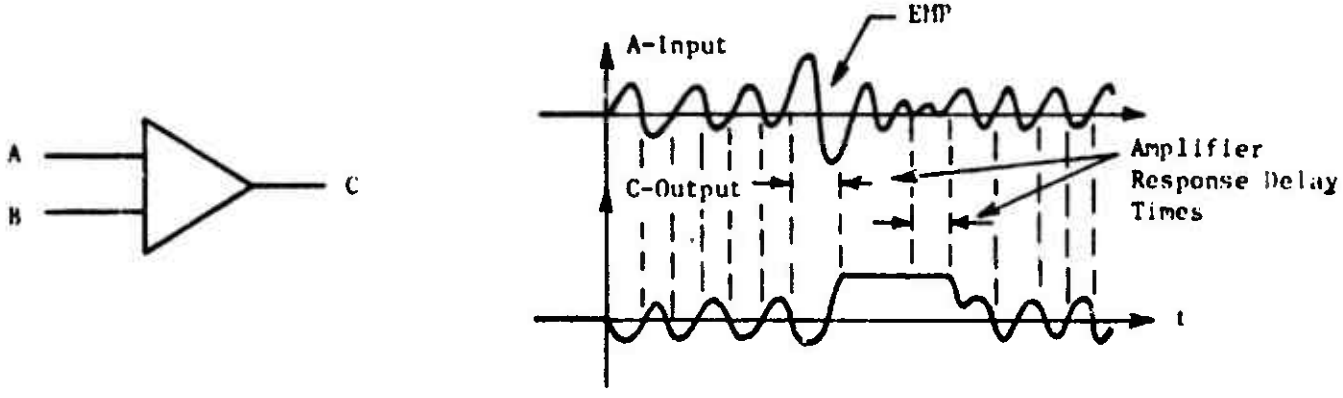
It should be noted that although these examples each postulate the appearance of transient at a specific input, the transients may appear at any combination of terminals. In some cases this "multiport" excitation may result in a lower upset threshold than that obtained for excitation of a single port.



(a) Flip-Flop Upset



(b) NAND Gate Upset



(c) Amplifier Upset

Figure I-3. Examples of Anomalous Circuit Response

d. Damage and Upset Commonalities

The approach used to reduce the EMP susceptibility problem from the system level to the circuit level is in itself quite involved and was summarized above to provide insight to the reader. This handbook does not deal further with this problem but rather presents detailed methods for determining circuit level damage and upset thresholds without regard to the rationale used in selecting a given circuit.

Once a specific circuit is identified, the next step is to either theoretically or experimentally determine the upset or damage thresholds of its sensitive ports. The basic steps in determining either upset or damage thresholds are as follows:

(1) Examine each circuit port for possible interest.

(2) If circuit vulnerability is to be assessed, define the source configuration (Z_s, V_{oc}) applicable to the port being analyzed.

(3) Select analysis method

- Hand Analysis
- Computer Analysis
- Experimental Analysis

(4) Obtain circuit component values and semiconductor device paramters.

(5) Perform analysis.

(6) Construct susceptibility matrix.

The susceptibility matrix referred to in Item (6) above is a matrix relating threshold data to circuit, subassembly, or subsystem injection points for use in selecting test monitor points or for evaluating hardening requirements. A detailed discussion of each step in the threshold analysis procedure is presented in Sections II and III for upset and damage respectively.

4. REFERENCES

The following references were used in this chapter.

1. Merewether, D. E., T. A. Cooper, K. L. Parker, et al, "Electromagnetic Pulse Handbook for Missiles and Aircraft In-flight," Sandia Laboratories, Albuquerque, New Mexico, September 1971.

2. Boeing Company, The, "Aeronautical Systems EMP Technology Review," AFWL Contract No. F29601-72-C-0028, Doc. No. D224-10004-1, April 1972.

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6. Boeing Company, The, "AABNCP Preliminary EMP Hardening Concepts," AFWL Contract No. F29601-72-C-0028, Boeing Document No. D224-10010-1, July 1972.

SECTION II

UPSET THRESHOLD ANALYSIS

1. GENERAL

The computation of the minimum signal level of specified time history that can cause a transient or nonpermanent degradation of a subsystem's functional capabilities, is called an Upset Threshold Analysis. An Upset Threshold Analysis is performed at the circuit level, after the circuits selected for analysis have been identified by a functional analysis, based on their criticality to the performance of subsystem functions. Since the concept of "Upset" is somewhat unique, the reader is encouraged to consider carefully the "Upset Considerations" portion of Section I.

Given that a specific circuit has been identified as being contributory to an upset problem, the computation of upset thresholds will proceed as follows:

(1) Obtain circuit data (i.e., component values, active device parameters, etc.) and analyze the circuit to determine the applicable operating mode (e.g., quiescent state).

(2) Examine each circuit node for possible interest.

(3) Select evaluation method:

  (a) Hand Analysis

  (b) Computer Analysis

  (c) Experimental Assessment

(4) Perform threshold analysia for selected nodes.

(a) Compute dc upaet threahold.

(b) Compute and plot threshold voltage or current aa a function of frequency.

(c) Enter data into ausceptibility matrix or computer data base.

(d) If vulnerability is to be assessed, determine the applicable driving function and source impedance. Vulnerability is determined by comparing the actual driving function to the reaults of (b).

For the purposes of this handbook, only interface circuit ports will be conaidered. Thia simplification assumes the use of good packaging and grounding techniques so that inadvertent intracircuit coupling is precluded. Thua, the analyst can asaume that the propagation of the EMP signal into the circuit occura only at ports that are connected directly to external cables. On the other hand, a less than optimal packaging deaign may allow cross talk between the interface and internal circuits in which case every circuit node must be analyzed and the problem is greatly magnified. While this handbook specifically addreasea interface porta, the analysis techniques presented apply to any circuit node.

2. RESPONSE CONSIDERATIONS

As stated previoualy, upaet may result from the anomalous response of either analog or digital circuitry. Howevar, experience has shown that tranaient effecta on digital circuits and data ia the most severe problem in that undesirable circuit disturbances occur at lower signal levels and a aingle logic level change can be transmitted throughout a logic system cauaing complex functional interactions. Furthermore, the technology involved (i.e., discrete component or integrated circuit) also influencea

the degree of the upset problem. Figure II-1 illustrates typical digital circuit upset threshold trends. The curves shown do not depict any particular digital circuit configuration, but rather show the relative upset levels associated with typical ac and dc coupled discrete and integrated digital circuits. Since most new systems use dc coupled, integrated circuit digital devices extensively, the balance of this section, including one of the example problems, is oriented towards this class of components.

Upset threshold analyses involve the use of conventional network and circuit analysis techniques, but present unique analytical problems for the following reasons:

(1) Spurious signals can appear at any interface port; therefore, circuits are excited in an abnormal manner.

(2) The frequency spectrum associated with an EMP stimulus is very broad; therefore, circuit response to unusually high frequencies must be determined.

The computation of upset thresholds for a given dc coupled digital circuit, therefore, involves the determination of voltage threshold as a function of frequency for every circuit interface port or, as a minimum, the computation of "worst case" (i.e., minimum threshold voltage and associated frequency). As shown in Figure II-1, the lowest upset threshold is the dc level. If the specified EMP signal does not exceed this voltage at any frequency, then the circuit will not be upset. Since the EMP signal amplitude is generally frequency dependent, the voltage threshold as a function of frequency should be determined. Therefore, there are two approaches to upset threshold analysis. First is the conservative approach which assumes the dc threshold to apply regardless of EMP frequency. As shown in Figure II-1, this approach could result in severe hardening penalties at high frequencies where the circuit upset threshold is actually much higher than the dc level. The second approach is to determine, either

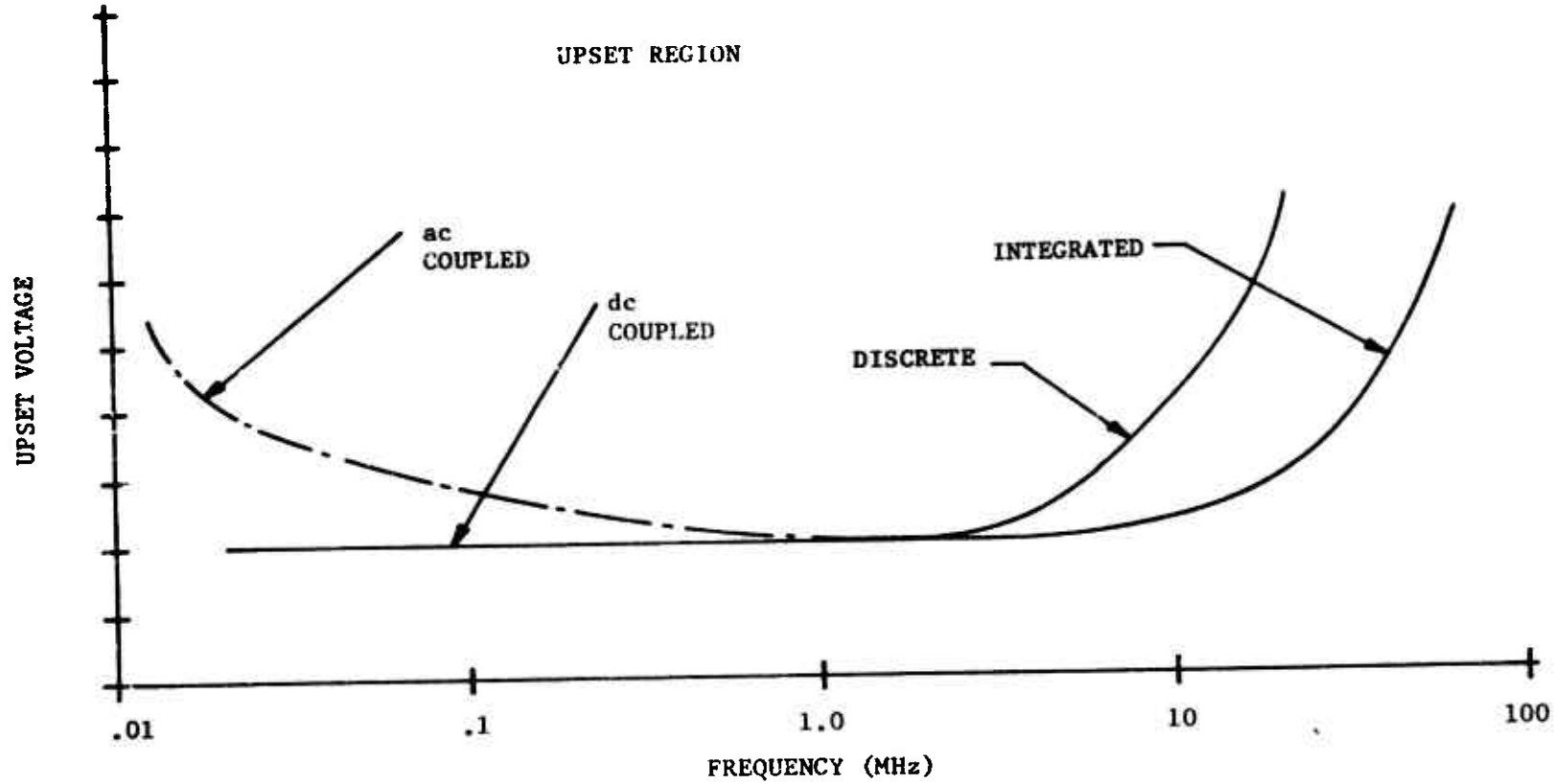


Figure II-1. Digital Circuit Upset Threshold Trends

experimentally or theoretically, the actual threshold voltage as a function of frequency. An approximate technique for calculating this relationship is presented below.

Tests have shown that for typical high gain switching circuits (References 1 through 4) transient upset is largely independent of the exact transient waveshape and depends only on the peak value of the transient and the time over which the transient exceeds the threshold. The high frequency knee of the curve shown in Figure II-1 occurs at a frequency related to the propagation delay time of the given circuit. Since the exact waveform of the applied transient is not critical, one can assume a rectangular pulse for simplicity. Since a damped sine wave cable response is often encountered, a relationship is required to relate a sine wave frequency to an equivalent rectangular pulse. The following relationship was derived empirically and found to give reasonable results:

$$f = \frac{1}{5t}$$

where

f = frequency of damped sinusoid
t = duration of rectangular pulse.

Based on the above information, the voltage threshold to cause circuit upset can now be evaluated as a function of t from an approximate energy relationship at the circuit node of interest:

$$E = \frac{V^2}{R} t$$

where

E = energy
V = voltage
R = input resistance
t = pulse duration

The minimum upset energy (E_m) is dependent on the propagation delay time (t_{pd}) and the dc threshold voltage (V_{dc}); therefore

$$E_m = \frac{V_{dc}^2}{R} t_{pd}$$

If one assumes that upset energy is constant, then the upset voltage for pulse durations shorter than t_{pd} may be determined as follows:

$$V_u^2 t_u = V_{dc}^2 t_{pd}$$

$$V_u = V_{dc}\left(\frac{t_{pd}}{t_u}\right)^{1/2}$$

where

V_u = actual upset voltage

t_u = actual pulse duration for $t_u < t_{pd}$

It should be emphasized that this is an approximate technique that neglects the frequency dependence and nonlinearity of circuit input impedance. This approach should be used only when the conservatism associated with the dc threshold level causes unacceptable hardening penalties. The results obtained using this method are compared with experimental threshold measurements on a flip-flop input port as part of the first example problem later in this section. Figure II-2 shows the results of this comparison. The predicted high frequency thresholds are lower than the measured thresholds and are therefore conservative.

As stated earlier, transient circuit upset may be caused by a signal coupled to any circuit node. Therefore, equal consideration must be given to normal input terminals, and any other circuit node exposed to transient injection. Since transients may be coupled to several circuit nodes simultaneously, the multiport response of each circuit must also be

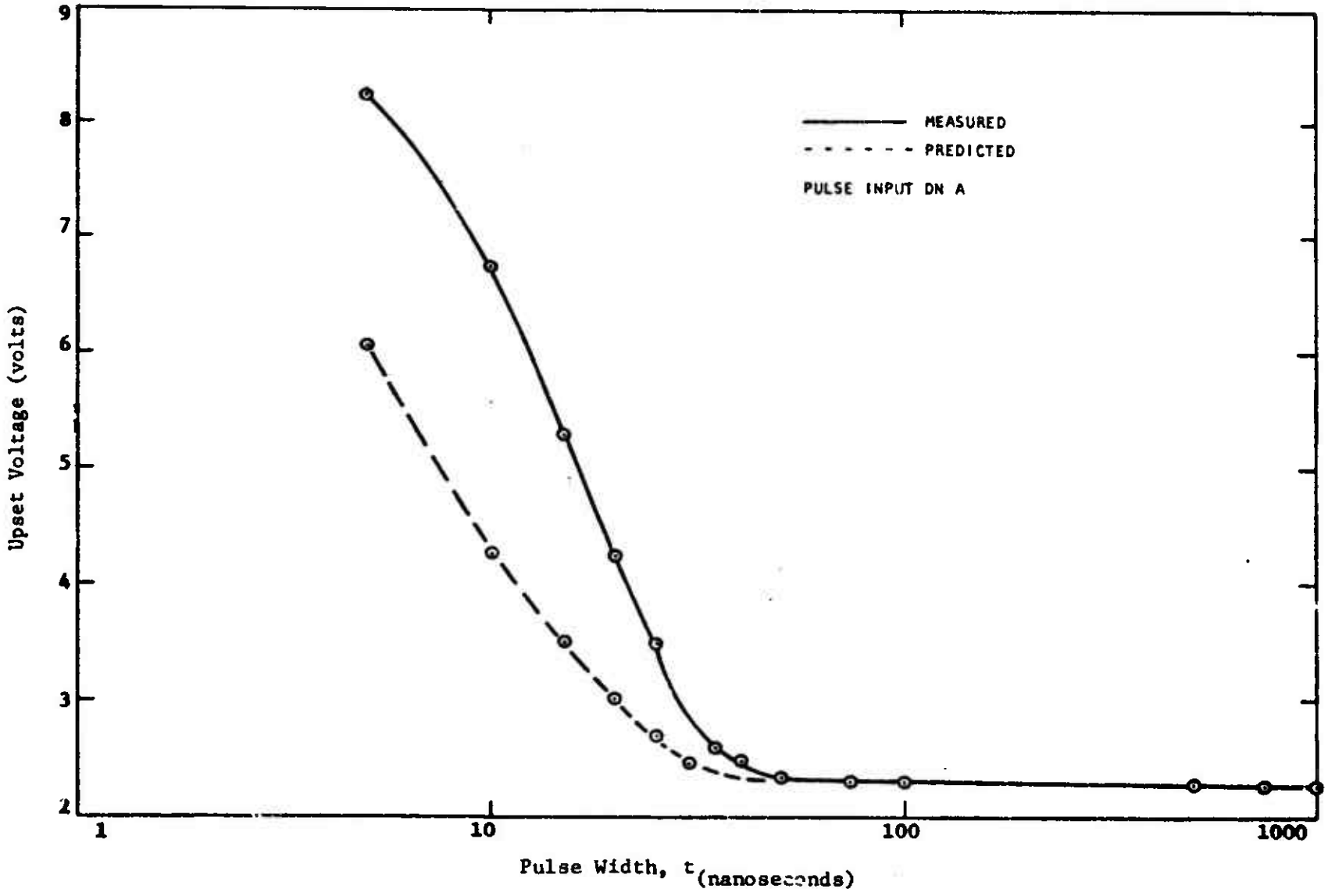


Figure II-2. Compsrison of Predicted and Measured Upset Levels for Short Pulse Durations

considered. For a given EMP field environment, the transient coupled to a given circuit node depends on the type and length of cable associated with the circuit and on the applicable EMP specification. Section IV discusses the evaluation of these factors. Unless the frequency, phase, and amplitude of the transients coupled to each circuit node are known, multiport response can be considered on a worst case basis only. As will be seen in the sample analyses presented later, the multiport cases considered did not yield significantly lower upset thresholds. Multiport upset studies have been performed by a few investigators (References 3 and 5), and upset thresholds lower than for the single port case have been reported in a few cases.

Once the transient upset threshold of each critical circuit node has been determined separately, the multiport response of the circuit should be estimated by inspection in order to determine if a detailed analysis is warranted.

3. ANALYSIS METHOD SELECTION

The three general approaches to upset threshold analysis are hand analysis, computer analysis, and experimental analysis. Each of these approaches has certain advantages and limitations which will be discussed below.

Hand analysis refers to the solution of a circuit problem by using simple computational aids such as a slide rule or simple electronic calculator. To determine a transient upset threshold using hand analysis requires the use of circuit analysis techniques such as Kirchoff's voltage and current laws, breakpoint techniques, and Driving Point Impedance Techniques (Appendix C).

The information required for hand analysis is the normal component values such as resistance, capacitance, inductance, and transistor or integrated circuit characteristics. In the case of semiconductors, the model used will depend on the circuit being analyzed. For an amplifier operating in its linear region, the hybrid pi or small signal h parameters can be used. For a digital or saturated switching circuit, large signal parameters such as turn-on time, turn-off time, and saturation voltages and logic truth tables are used. This information is normally available from manufacturer's data sheets. In the case of saturating digital circuits, much information can be gained by a "quick-look" analysis using only the logic truth table and the logic levels of the gates of interest. This method will be used later in one of the sample hand analyses.

Computer analysis refers to the use of one of the available transient analysis computer codes (CIRCUS 2, NET-2, SCEPTRE, etc.) to solve a given circuit problem. The available computer codes vary in applicability from the very simple, capable of handling a several node problem, to the extremely complex with capability for kilonode problems. Since there are many user oriented circuit analysis computer codes available, the selection of a particular code is best made on the basis of availability and user familiarity. The sample computer-aided circuit problems presented in this handbook were performed using CIRCUS 2, NET-2, and SCEPTRE.

Experimental assessment of a circuit's transient upset threshold refers to the direct injection of a signal at one or more ports and the measurement of signal level required to produce circuit upset. Given available laboratory facilities and a well defined circuit problem, experimental determination of transient upset levels can be an accurate and cost effective approach.

The selection of a particular analysis method depends on the objective of the analysis and must take into account the following factors:

(1) Circuit complexity - This refers to the number of active and passive components, voltage sources, and current sources.

(2) Problem complexity - This refers to the number of solutions required and the number of variables to be considered. Variations in problem complexity depend directly on the complexity of the EMP specification and therefore on the source configuration and driving function complexity. This factor is therefore related to the circuit vulnerability assessment.

(3) Data required - This refers to the circuit component values and device characteristics that must be known to solve a given problem. The data required vary considerably depending on whether discrete or integrated circuits are being considered and upon the particular analysis method being used.

(4) Accuracy required - Since the objective of a transient upset analysis is to determine the relative upset thresholds of varying types of circuits, the precision of the upset voltage levels calculated is not too critical.

(5) Economy - If one or more analytical techniques yield comparable results, the time and cost of analysis should be considered.

(6) Number of similar analyses to be performed - If several similar circuits are to be analyzed, the selection of an analysis technique should be made so that duplication of computation is minimized.

Figure II-3 is an analysis technique selection matrix that weights the three analysis techniques based on the six selection factors just described. Depending on the importance of each selection factor for a given problem, the three analysis methods are numbered 1, 2, and 3 in order of preference; therefore, the lowest cumulative weighting indicates the preferred method. An analysis technique can be selected accordingly. Separate matrices are presented for discrete component and integrated circuits. Figure II-3 shows clearly that each analysis technique has its advantages and limitations. Considering all six analysis technique selection factors, the experimental method is found to have an overall advantage. The weighting of individual selection factors is admittedly subjective, but the concluaion that experimental determination of upset thresholds is most practical has been found to be valid in many instances. This concluaion is not intended to be general, and users of this analysis technique selection approach should evaluate the nature and objective of their particular upaet problem and fill out the matrix accordingly.

Hand analysis, computer aided analysis, and experimental assessment of transient circuit upset thresholds, properly utilized, will yield comparable results. Sample problems presented later illustrate the equivalence of computational accuracy of the three methods and therefore show that accuracy is not a primary consideration for most problems.

The experimental determination of a circuit's upset characteristics is a reasonably straightforward procedure requiring only adequate laboratory facilities and carefully prepared test plans. If the transient threshold characteristics of a large number of reasonably simple circuits are required, an experimental program may not be practical. In this event, hand analysis provides a fast and straightforward means for determination of dc upset characteristics. For the simple circuit case, computer-aided analysis may not be practical due to the time required to accumulate device parameters, to format the circuit, and to debug the input deck. Computer-aided analysis provides the best means for determining the transient upset thresholds of a

SELECTION FACTORS / TYPES OF ANALYSIS	DISCRETE CIRCUITS							INTEGRATED CIRCUITS						
	CIRCUIT COMPLEXITY	PROBLEM COMPLEXITY	DATA REQUIRED	ACCURACY REQUIRED	ECONOMY	NUMBER OF SIMILAR ANALYSES	TOTAL	CIRCUIT COMPLEXITY	PROBLEM COMPLEXITY	DATA REQUIRED	ACCURACY REQUIRED	ECONOMY	NUMBER OF SIMILAR ANALYSES	TOTAL
HAND	2	3	2	-	1	3	11	2	3	2	-	2	2	11
COMPUTER	1	2	3	-	3	1	10	3	2	3	-	3	3	14
EXPERIMENTAL	3	1	1	-	2	2	9	1	1	1	-	1	1	5

Figure II-3. Transient Upset Analysis Technique Selection Matrix

large number of similar circuits or of circuits containing or being driven by sources having reactive elements. The practicality of using one of the transient analysis circuit codes is very dependent on the size and accuracy of the semiconductor device library available.

Whether hand analysis or computer-aided analysis is used to solve a given transient upset problem, verification of the results using experimental techniques is often required. Given a firm guideline such as the B-1 common mode cable current specification, simplifying assumptions, such as the use of dc thresholds, may be made that make the use of hand analysis techniques advisable in order to obtain usable results in a minimum amount of time.

4. DATA REQUIRED FOR UPSET ANALYSIS

Theoretical transient circuit upset analysis is performed in two steps: first, the dc upset threshold of each selected circuit node is determined; second, the frequency dependence of each circuit node upset threshold is determined if the driving function frequency is a factor. Since the dc upset threshold represents the worst case for any port, the sample analyses presented in the next section emphasize the determination of this voltage level. An approximate method for determining the threshold at a specific frequency, given the dc upset level, was presented earlier for general reference and is demonstrated by the first example problem.

Limiting analysis to the dc threshold case minimizes the data required in order to assess a given circuit. For hand analysis, the dc upset threshold for either integrated or discrete circuits can be determined using passive component values and data directly from manufacturer's specifications. Detailed component data are not generally available for integrated circuits, thus, the logic circuit levels given by the manufacturer, combined with the known switching characteristics of silicon

transistors, can be used to estimate the dc upset thresholds of various circuit nodes. Since most existing transient analysis codes use a specific model for semiconductor devices (Ebers-Moll, charge control, etc.), more device data may be required to utilize a given computer code than is required for hand analysis. If considerable use of computer codes for the determination of circuit dc upset thresholds is planned, simplified piecewise linear models should be developed in lieu of more complex models. Some of the device models available for use in upset analysis are discussed in Appendix A. The computer-aided analysis of integrated circuit dc upset thresholds is not presently practicsl because of the lack of circuit element data on most manufacturers' specifications. The development of simplified modeling techniques for integrated circuits (References 6 and 7) will greatly assist in studying IC upset, but at the present time, this approach is still unproven. The first circuit upset problem presented later in this section shows that hand analysis is reasonably straightforwsrd for the IC case.

By limiting upset analysis to the dc threshold case, the circuit and device parameters that contribute to circuit response or propagation delay time need not be known. The analysis problem is not trivial however, since the dc thrssholds of all ports must be calculated for both positive and negative polarities.

5. UPSET ANALYSIS EXAMPLES

a. Hand Analysis

The method used to dstarmine the upset threshold of a given circuit will, to a large extent, be determined by the informatlon availabla on that circuit and on the complexity of the circuit. There is little circuit simplification that can be done for upset since the circuit is normally in the "power-on" condition and sll components are interacting.

For logic or saturated switching circuits one can first establish a truth table for the circuit and examine this truth table for upset conditions. The next step is to examine the schematic diagram and to consider the effects of transients of either polarity on the susceptible ports. (The dc upset levels are assumed to be the dc logic levels.) The frequency dependence is then determined using a relationship like the one derived earlier in this section.

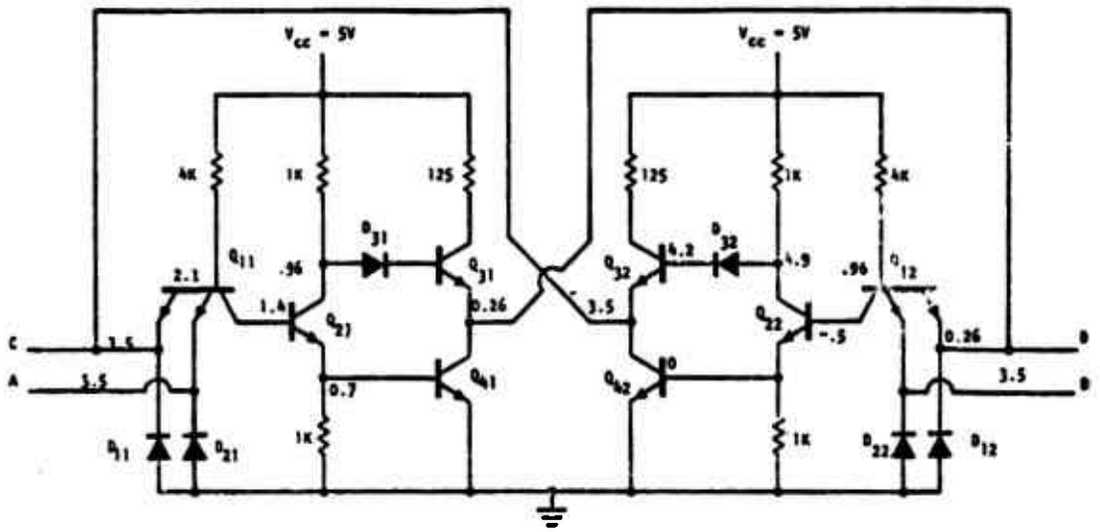
The following two examples have been chosen as representative of the types of analyses that are required to compute circuit upset thresholds. The first problem involves an integrated circuit flip-flop consisting of cross-coupled TTL NAND gates. The analysis for this circuit is based on the truth table for the circuit and a "quick look" method involving only information available from the manufacturer's data sheet.

The second analysis is a detailed analysis of a discrete component flip-flop. Many of the techniques that could not be applied to the integrated circuit case are used since component parameters were available for all semiconductors. The discrete flip-flop was also analyzed using SCEPTRE, NET-2, and CIRCUS 2, and the results of the computer-aided analysis are discussed later in this section.

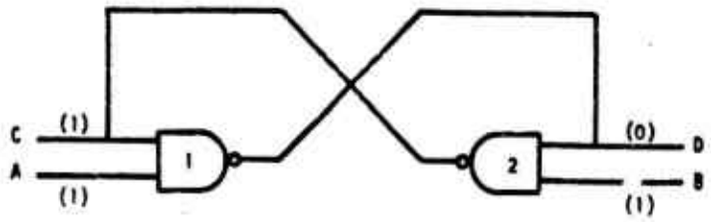
(1) Problem 1. Integrated Circuit Flip-Flop

As one example of using hand analysis methods to determine upset thresholds, consider an R-S flip-flop utilizing a pair of cross coupled, integrated circuit, 2-input NAND gates. To fully show the analysis methodology, it is assumed that a transient signal can appear on any line connected to the circuit.

A schematic diagram of the flip-flop is shown in Figure II-4a and a logic diagram of the flip-flop is shown in Figure II-4b. Also



(a) Schematic Diagram



(b) Logic Diagram

Figure II-4. Integrated Circuit Flip-Flop

shown in Figure II-4b are the logic states at each terminal for one of its two stable states. The inputs, A and B, are normally held at a logic "1" and require a negative going pulse (to logic "0") to trigger the circuit. The outputs of this circuit are C and D. Figure II-5a describes the normal operation of the flip-flop. The quiescent state shown in Figure II-4 (A = "1" and D = "0" and B = "1") will be used in this analysis. Results for the other state can be obtained by interchanging A with B and C with D.

A specification sheet for the type of TTL logic used in this analysis is shown in Figure II-5b. Detailed component data are generally not available for IC's. Using only the information from the data sheet, one can approximately determine the voltages at various points in the circuit. These voltages are shown on the schematic in Figure II-4.

The quiescent point analysis of the circuit shown in Figure II-4 is an approximation based on typical transistor performance characteristics. From the specification sheet, the logic "0" output voltage is 0.26 volt. By looking at the schematic, this voltage would appear to be the $V_{CE\ sat}$ of the output transistor. Since these are silicon devices, $V_{BE\ sat}$ can be assumed to be 0.7 volt. A typical value of logic "1" voltage is listed as 3.5 volts. Using these values and the logic state shown in Figure II-4, one can establish that inputs A and B, output C, and Q_{42} collector are at 3.5 volts. Output D and Q_{41} collector are at 0.26 volt. Since Q_{41} is saturated, the base voltage is 0.7 volt which indicates that Q_{21} is also in saturation. The voltage at the base of Q_{21} is therefore 1.4 volts and the voltage at its collector is 0.96 volt. The voltage between the collector of Q_{21} and the emitter of Q_{31} (0.7 volt) is insufficient for saturation of both dioda D_{31} and the emitter base junction of Q_{31}, therefore Q_{31} is cut off. With Q_{21} and Q_{41} both saturated, the collector-base junction of Q_{11} is forward biased. The voltage at the base of Q_{11} is therefore 2.1 volts and the emitter-base junctions are both reverse biased.

Input Pulsed	t_o				$t_{n+\Delta}$			
	A	B	C	D	A	B	C	D
A → 0	1	1	1	0	1	1	0	1
B → 0	1	1	1	0	1	1	1	0
A → 0	1	1	0	1	1	1	0	1
B → 0	1	1	0	1	1	1	1	0

NOTE: t_n = time before pulse application

$t_{n+\Delta}$ = time after end of pulse

(a) Flip-Flop Truth Table

ABSOLUTE MAXIMUM RATINGS

	Military	Industrial	Unit
Supply Voltage	8	7	Vdc.
Operating Temperature	-55° to +125°	0° to +75°	°C
Storage Temperature	-65° to +200°	-65° to +200°	°C

ELECTRICAL CHARACTERISTICS AT 25° C, Vcc=5V

Input Characteristics	Min.	Typ.	Max.	Unit
Logic 1 Voltage	1.7		5.5	Volts
Logic 1 Current			100	μA
Logic 0 Voltage			1.2	Volts
Logic 0 Current		1.0		mA
Capacitance		2.0		pF
Positive Noise Immunity	1.0			Volts
Negative Noise Immunity	1.0			Volts
Frequency		20		MHz
Output Characteristics	Min.	Typ.	Max.	Unit
Logic 1 Voltage	3.0	3.5	3.8	Volts
Logic 0 Voltage		0.26	0.45	Volts
Short Circuit Output Current	10		45.0	mA
Propagation Delay Time/Gate (varies with element designed to be used up to 20 MHz)		10	20	ns

(b) NAND Gate Specifications

Figure II-5. Integrated Circuit Flip-Flop Characteristics

Since one of the emitters of Q_{12} is low, the emitter-base junction of Q_{12} is forward biased and the voltage at the base of Q_{12} is 0.96 volt. For Q_{42} and Q_{22} to be saturated and the collector-base junction of Q_{12} to be forward biased would require the voltage at the base of Q_{12} to be 2.1 volts. Because the voltage at the base of Q_{12} is much less than this, Q_{22} and Q_{42} are cut off. The voltage at the collector of Q_{22} is therefore approximately 4.9 volts. This is sufficient to forward bias the diode D_{32} and the emitter-base junction of Q_{32}. Q_{32} is therefore on and the voltage at its base is 4.2 volts.

Initially, the analysis will be for pulse widths much longer than the propagation delay of the circuit. This is approximately 40 ns or twice the maximum delay time of one gate. As discussed earlier, this will give the dc upset level for each circuit port. Upset thresholds for higher frequencies will be discussed later.

Table II-1 is a summary of the possible upset modes for this circuit including a comparison of predicted and measured dc threshold voltages. Each case is discussed below.

Case 1 - Input A

(a) A positive going signal on A will not change the state of D so no upset will occur. There is the possibility of damage to diode D_{21} or to the emitter-base junction of Q_{21} once their breakdown voltage is exceeded ($\sim$ 7 V).

(b) A negative going signal on A will cause the circuit to change state. A signal that drives A to below its maximum logic "0" level ($\sim$ 1.2 V) will cause D to change to a logic "1" (normal NAND function), the change on D will cause C to change to a logic "0" (also a normal NAND function). The flip-flop has therefore upset, the upset threshold being the difference between the logic "1" and logic "0" levels (3.5 - 1.2) or approximately 2.3 volts.

TABLE II-1

COMPARISON OF PREDICTED AND MEASURED UPSET LEVELS FOR INTEGRATED CIRCUIT FLIP-FLOP

Upset Case	Terminal Pulsed	Pulse Polarity	Upset Level	
			Predicted (Volts)	Measured (Volts)
1(a)	A	+	*	*
1(b)	A	–	2.3	1.7
2(a)	B	+	3.5	6.0
2(b)	B	–	*	*
3(a)	C	+	*	*
3(b)	C	-	2.3	2.0
4(a)	D	+	1.7	1.7
4(b)	D	-	*	*
5(a)	V_{cc}	+	*	5.5**
5(b)	V_{cc}	-	5.0**	5.5**
6(a)	Gnd	+	5.0**	7.0**
6(b)	Gnd	-	*	5.0**

NOTES: *No Upset
**Final State is the preferred state.

Case 2 - Input B

(a) A positive going signal on B could cause an upset if the breakdown voltage of the emitter-base junction of Q_{12} is exceeded (~7 V). Once this voltage is exceeded, the voltage on the base of Q_{22} would increase turning it and Q_{42} on. Output C would change to logic "0" which in turn will cause D to go to logic "1" and the circuit is upset. The transient signal required is the difference between the breakdown voltage of the emitter-base junction of Q_{12} and the normal logic "1" input voltage (7.0 - 3.5) or approximately 3.5 volts.

(b) A negative going signal on B will not cause upset. This signal will not cause an output change. There is a possibility of damage if B goes highly negative due to a large forward bias on D_{22}.

Case 3 - Output C

(a) This analysis is the same as Case 1 (a).

(b) This analysis is the same as Case 1 (b).

Case 4 - Output D

(a) A positive going signal on D will cause the circuit to change state. A signal that drives D above the minimum logic "1" level (~1.7 volts) will cause C to go to logic "0" (normal NAND function). Since A is logic "1" and C is logic "0," D will be held at logic "1" and the flip-flop has been upset. The transient signal amplitude required is the minimum logic "1" level of 1.7 volts.

(b) A negative going signal on D will not cause upset but may result in permanent damage to forward biased diode D_{12}.

Cases 5 (a) (b) and 6 (a) (b) - Power Supply and Ground Lines

For this circuit, the results of a transient on the power supply and ground line are for the most part, indeterminate. Due to variations in component values, the circuit will normally have a preferred state. If the circuit is to upset, it will generally go to this state. A few general statements can be made about upset due to power supply and ground line transients. A negative going transient on the power supply line (~5 V) will cause the flip-flop to go to its preferred state. This is the same as turning off the supply voltage and then turning it on again. The same is true for a positive going transient on the ground line.

The upset threshold voltages for this circuit are the voltages at the ports. Since these voltages are small and the currents involved are on the order of 10 ma or less, the magnitude of the source impedance will have little effect on generator voltage required for upset.

An integrated circuit flip-flop of the type just described was tested to verify the predicted upset levels. A comparison of the predicted and measured values are shown in Table II-1. Upset occurred in all predicted cases. Upset also occurred when positive going pulses were injected on the power supply and ground lines. In both cases, the final flip-flop state was the preferred state. While these cases were not predicted, the upset is due to the negstive voltage excursion that occurs at pulse termination. This negative "overshoot" is due to circuit charge storage tendencies and gives effectively the same results as does a negative pulse.

Upset can occur for pulse widths shorter than the propagation delay time of the flip-flop. However, as discussed earlier, as the pulse duration becomes shorter, the pulse amplitude required for upset becomes lsrger. The expression derived in Section II.2 can be used to compute the upset threshold for any frequency (or pulse width) given the dc value.

A comparison of the predicted and measured upset thresholds for various frequencies was shown in Figure II-2 and is repeated here for reference only. The data given in this figure apply to input A. The expression used to compute the upset voltage at various frequencies is:

$$V_u = V_{dc}\left(\frac{t_{pd}}{t_u}\right)^{1/2}$$

where

t_{pd} = 40 nsec

V_{dc} = 2.3 volts

t_u = pulse duration

V_u = computed threshold voltage at t_u.

As was indicated earlier, the estimate of the upset voltage for higher frequencies is only sn approximation and the technique used has not been studied sufficiently to allow confidence in its general applicability. Since the worst case upset threshold is the dc value, the high frequency threshold approximation is not critical to a hardening effort.

(2) Problem 2. Discrete Transistor Flip-Flop

The discrete transistor flip-flop (bistable multivibrator) shown in Figure II-6 was chosen for "upset" analysis by both hand and computer methods. Transistors Q_5 and Q_6 comprise the basic flip-flop stage and transistors Q_4 and Q_7 act ss output buffer stages. Negative input signals are applied to IF-01 and the OF-01 terminals to "set" and "reset" the circuit, respectively. Diodes D_1 and D_2 cause the inputs normally to respond only to negative trigger signals. Diodes D_7 and D_8 prevent the bases of Q_5 and Q_6 from going more positive than a single diode drop due

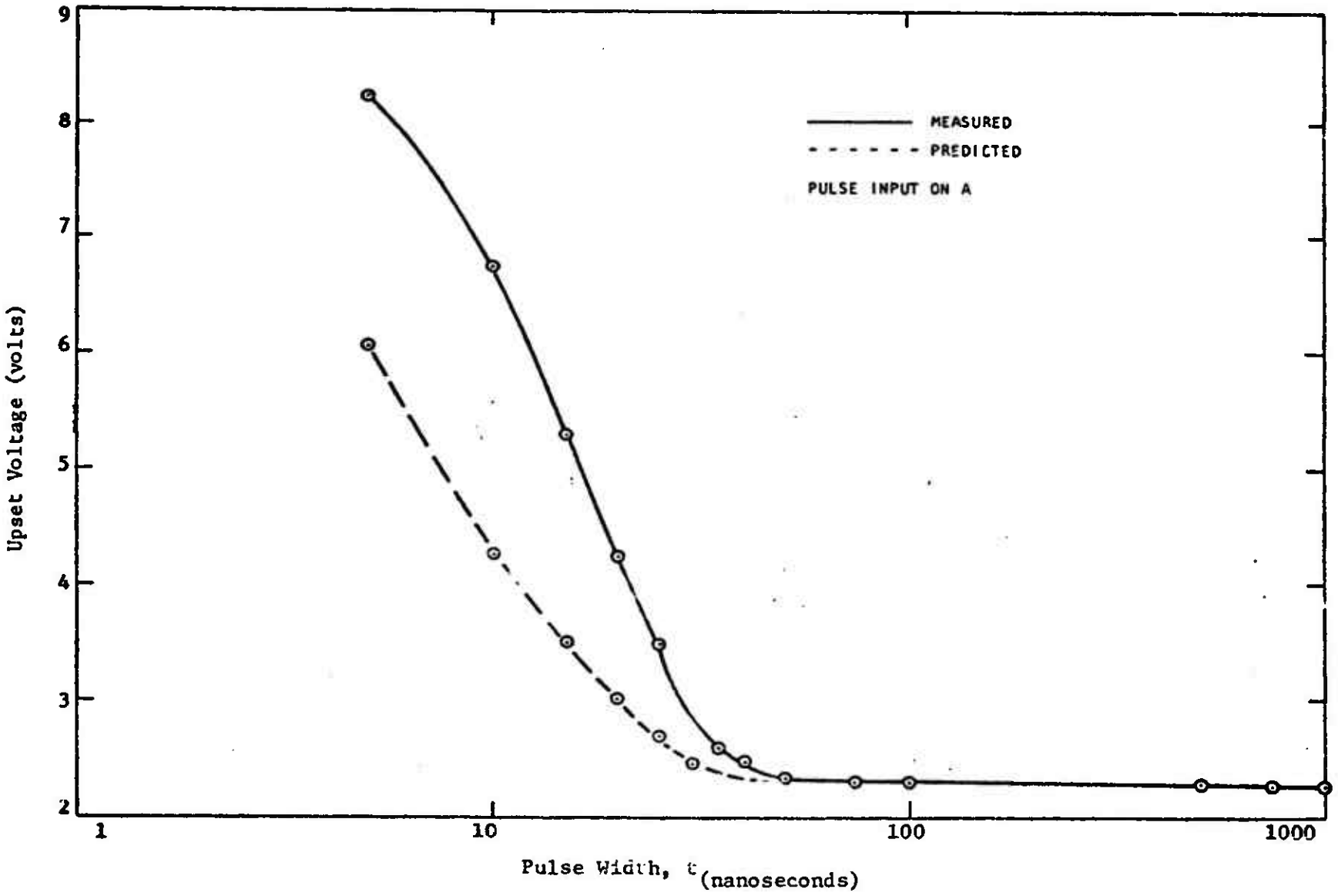


Figure II-2. Comparison of Predicted and Measured Upset Levels for Short Pulse Durations

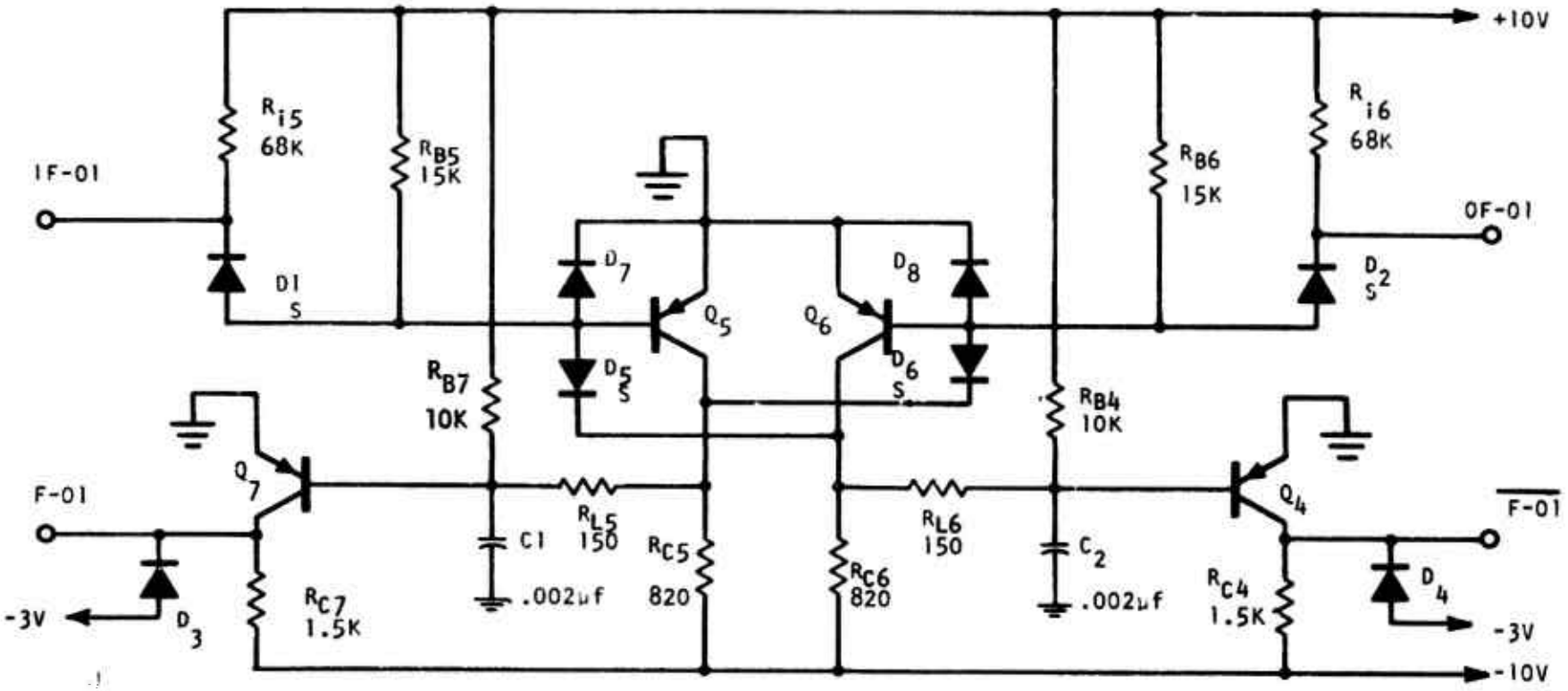


Figure II-6. Schematic Diagram of Discrete Component Flip-Flop Circuit

to currents through biasing resistors R_{B5} and R_{B6}. Cross-coupling diodes D_5 and D_6 prevent the collector of the "off" transistor from going more negative than about -0.9 volts (represents base-emitter drop of "on" transistor, ≈ 0.3 V, plus silicon diode drop of ≈ 0.6 V). The R_{L5} C_1 and the R_{L6} C_2 networks reduce the speed of the circuit and cause the output buffer stages to be more immune to noise transients. The outputs F-01 and $\overline{\text{F-01}}$ at the collectors of the buffer stages, Q_4 and Q_7, are prevented from going more negative than -3 volts by the collector catching (limiting) diodes D_3 and D_4.

Only diodes D_1, D_2, D_5, and D_6 are silicon devices (indicated by S); all the remaining diodes and transistors are germanium devices. The nominal collector voltage of a saturated germanium transistor is assumed to be -0.1 volt, and the forward-biased base-emitter junction is assumed to be -0.3 volt. The forward drop across the silicon diodes is assumed to be +0.6 volt, whereas the forward drop across the germanium diodes is assumed to be +0.3 volt. Using these values of voltsges across "on" and/or "saturated" diodes and transistors as a starting point, one proceeds through the circuit employing Kirchoff's and Ohm's Laws to find the approximate magnitudes of all circuit currents and voltages.

If we consider the flip-flop consisting of Q_5, Q_6, and associated circuitry to be in the "reset" condition with Q_6 "on" and saturated (assuming positive potential logic), we know that the base potential of Q_6 should be -0.3 volt and its collector potential should be -0.1 volt. Under this reset condition, Q_5 will be "cut off" and the buffer output stages Q_4 and Q_7 will be in the "cutoff" and "on" states, respectively. Continuing, with only $V_{BE6} \approx -0.3$ volt and $V_{CE6} \approx -0.1$ volt assumed known, the currents and voltages throughout the remainder of the circuit are found by Kirchoff's and Ohm's Laws as follows:

$$I_{R_{C6}} = \frac{10-V_{CE6}}{R_{C6}} = 12.06 \text{ ma}$$

$$I_{R_{B4}} = \frac{10+V_{CE6}}{R_{B4}+R_{L6}} = 0.995 \text{ ma}$$

$$V_{B4} = 10\left(\frac{R_{L6}}{R_{B4}+R_{L6}}\right) - V_{CE6}\left(\frac{R_{B4}}{R_{B4}+R_{L6}}\right) = 0.0491V$$

$$I_{C6} = I_{R_{C6}} - I_{R_{B4}} = 11.065 \text{ ma}$$

$$I_{R_{B7}} = \frac{10 + V_{BE7}}{R_{B7}} = 1.03 \text{ ma}$$

$$I_{R_{L5}} = \frac{V_{CE5} - V_{BE7}}{R_{L5}} = 4.0 \text{ ma}$$

$$I_{B7} = I_{R_{L5}} - I_{R_{B7}} = 2.97 \text{ ma}$$

$$I_{R_{C7}} = \frac{10 - V_{CE7}}{R_{C7}} = 6.6 \text{ ma}$$

$$I_{R_{B6}} = \frac{10+V_{BE6}}{R_{B6}} = 6.88 \text{ ma}$$

$$I_{R_{C5}} = \frac{10-V_{CE5}}{R_{C5}} = 11.1 \text{ ma}$$

$$I_{D6} = I_{R_{C5}} - I_{R_{L5}} = 7.1 \text{ ma}$$

$$I_{B6} = I_{D6} - I_{R_{B6}} = 0.22 \text{ ma}$$

$$I_{R_{B5}} = \frac{10-V_{BE5}}{R_{B5}} = 0.647 \text{ ma}$$

$$I_{R_{C4}} = \frac{10-V_{CE4}}{R_{C4}} = 4.47 \text{ ma}$$

Thus, we have found the nominal voltage and current values expected in the circuit by assuming only the base and collector voltages of the saturated transistors and the diode drops across the forward-biased diodes. The terminal voltages and the state of the various transistors are:

$V_{B6} = -0.3V.$	$V_{B5} = +0.3V$
$V_{C6} = -0.1V$	$V_{C5} = -0.9V$
SAT	CUTOFF
$V_{B4} = +0.0491V$	$V_{B7} = -0.3V$
$V_{C4} = -3.3V$	$V_{C7} = -0.1V$
CUTOFF	SAT

Assuming that the breakpoint voltages of silicon diodes occur at 0.6 volt and zero current, the base-emitter breakpoint of the germanium transistors occurs at -0.3 volt and zero current, and the breakpoint of germanium diodes occurs at +0.3 volt and zero current, we may analyze the circuit for possible threshold triggering levels. Although these trigger levels are essentially dc levels, they will apply to this circuit for pulses of duration which are long compared to the propagation delay of the circuit.

For triggering of the flip-flop to occur, a signal must appear on the IF-01 terminal which will carry the base of Q_5 from +0.3 V to -0.3 V or a total change at the input of -0.9 volt (if E_i begins at zero, it must go negative to -0.6 V in order to carry V_{B5} to zero; and then, it must go to -0.9 V to carry V_{B5} to -0.3 V; therefore, $\Delta E_i = -0.9$

volt. This indicates that the minimum threshold voltage to trigger or to "upset" is -0.9 volt).

In order for the circuit to switch with a transient input on IF-01 which equals or exceeds the threshold of -0.9 V, the pulse duration (T_1) must exceed a given minimum value which is determined by the circuit's pulse response. In other words, the E_i input must trigger Q_5 "on" sufficiently long for Q_6 to come out of saturation and propagate a feedback signal through D_5, which will ensure that Q_5 will remain in the conducting state when the E_i pulse terminates. An estimate of this minimum pulse duration can be made by utilizing transistor specification sheet data and circuit parameters given on the circuit diagram.

An additional condition must be satisfied, of course, if switching is to be possible at all; that is, the "loop-gain," when both Q_5 and Q_6 are active, must exceed "unity." The greater-than-unity loop gain requirements are always necessary for the trigger circuit to function and they must be satisfied in the initial design; however, it is appropriate to consider the minimal transistor parameters which can be tolerated before the circuit becomes completely inoperative. For the circuit under consideration, these minimum transistor parameters are determined by writing the "loop gain" of the circuit as follows.

Refer to the equivalent circuit shown in Figure II-7. The identity of transistors Q_5 and Q_6 are retained; however, it is assumed that both D_5 and D_6 are forward biased during the switching transient and they have been replaced by r_{d5}, the forward resistance of D_5, and r_{d6}, the forward resistance of D_6. Capacitors C_1 and C_2 are shown on the equivalent circuit diagram; however, they are considered as signal short circuits during the switching transient.

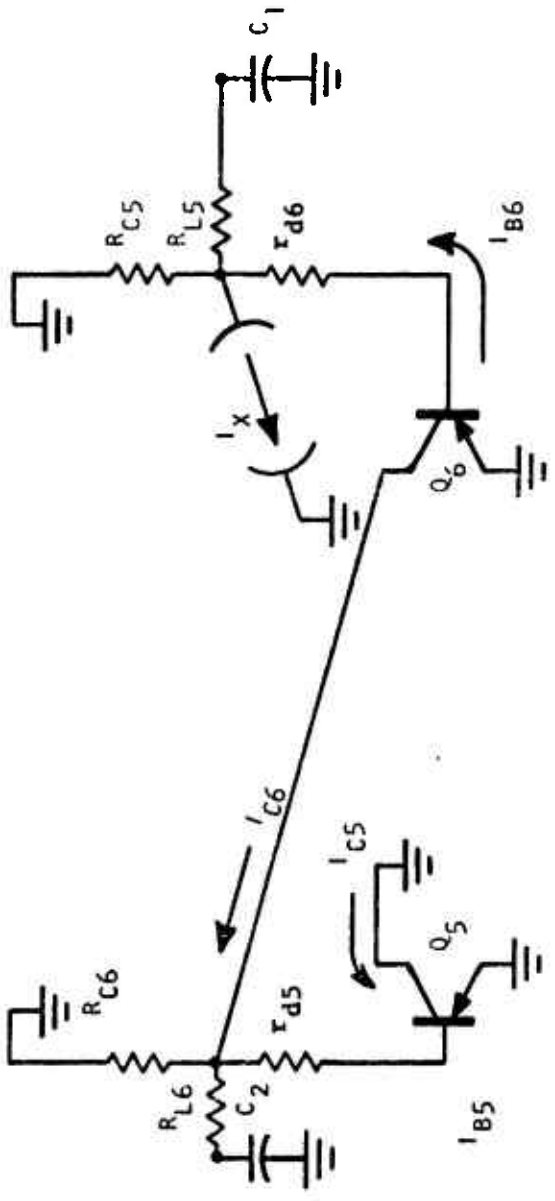
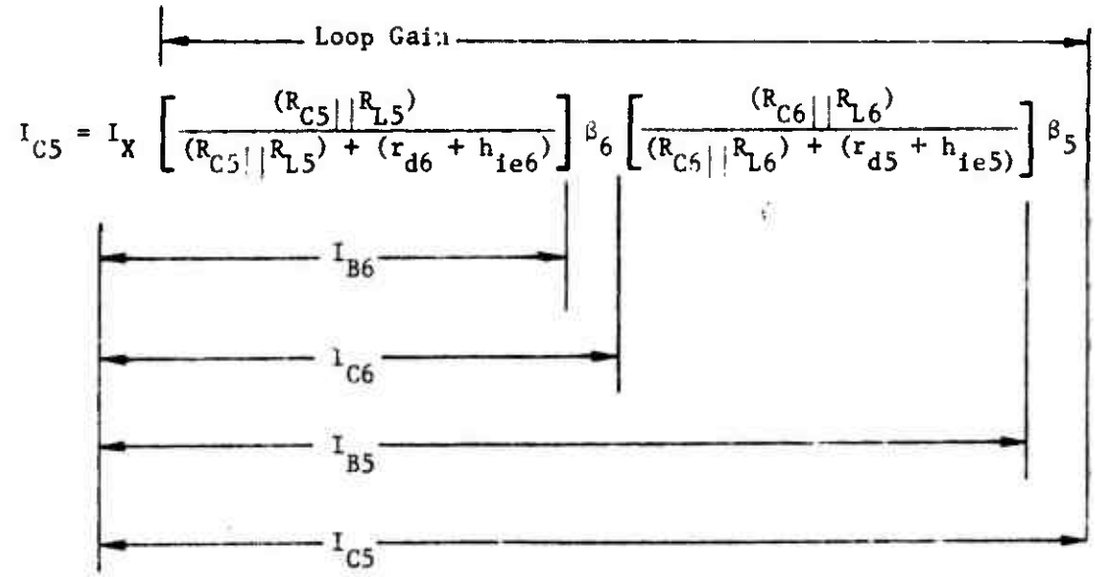


Figure II-7. Equivalent Circuit of Flip-Flop During Switching

The DPI technique for determining "loop gain" is to break the loop at the collector of Q_5 and insert independent current generator I_x between the $R_{C5} - R_{L5} - r_{d6}$ node and common ground.* The loop can be broken at other locations, but the circuit break must be properly terminated in both directions; breaking the loop at a transistor's collector terminal alleviates the necessity of terminations. The "loop gain" of the circuit shown in Figure II-7, written out by inspection using DPI techniques, is



$$G_{LOOP} = \frac{I_{C5}}{I_X} = \left[\frac{(R_C||R_L)}{(R_C||R_L) + (r_d + h_{ie})}\right]^2 \beta^2$$

*In effect, this technique represents the replacement of the single $\beta_5 I_{B5}$ current generator with a series combination of two identical current generators whose magnitudes are given as $\beta_5 I_{B5}$ and I_x, respectively. The newly created node between the two current generators is then grounded, but since $\beta_5 I_{B5}$ must identically equal I_x, this new node can be connected to any arbitrary point (the current into the new node exactly equals the current out of the node). With the new node at ground, I_x is assumed independent initially and the value of the $\beta_5 I_{B5}$ generator is calculated as a function of I_x and all other input signals. The dependent $\beta_5 I_{B5}$ generator is then set identically equal to I_x, thus reestablishing the feedback loop. Loop gain is defined as $[\beta_5 I_{B5} = f(I_x)] \div I_x$ before feedback is reestablished.

The loop gain expression implies that

$$\beta \geq \left[\frac{(R_C || R_L) + r_d + h_{ie})}{(R_C || R_L)}\right]$$

if loop is to exceed unity.

After the quiescent dc potentials have been computed and the normal trigger levels determined (ΔE_i = -0.9 V as shown above), it is advisable to make a table of all possible single input transient conditions and to determine how these transients affect the circuit operation. Inputs IF-01, $\overline{\text{F-01}}$, and the -10 volt buss of the circuit shown in Figure II-6 were chosen for studying "upset." The various cases to be considered are systematically listed in Table II-2. Note that each case is assigned a number and that both positive and negative transient input signals are considered for each possible state of the flip-flop. Although some of the cases may represent trivial conditions, they should each be systematically investigated so that no case will be overlooked.

Case 1 (a) Positive Input IF-01 with Q_5 On

At approximately e_i = +75 volts,* diode D_1 (FD-600) will break down, couple the input signal into the base of Q_5, and cause the circuit to change states. Therefore, this is an "upset" condition. If the input current rises considerably, diode D_7 will be in the conducting state and it is possible for diode D_5 to forward bias and pull Q_4 out of conduction which also represents an "upset" condition (but Q_4 would have already gone into the "off" state when Q_5 changed state).

*The spec sheets for the FD-600 diode show that reverse current is beginning to increase rapidly at ≈+60 V; therefore, +75 V is chosen as the approximate V_{BD}.

TABLE II-2

SUMMARY OF POTENTIAL UPSET MODES

CASE	PULSE POLARITY	TERMINAL PULSE	CIRCUIT STATE
1 (a)	+	IF-01	Q_5 On
1 (b)	-	IF-01	Q_5 On
2 (a)	+	IF-01	Q_5 Off
2 (b)	-	IF-01	Q_5 Off
3 (a)	+	$\overline{\text{F-01}}$	Q_5 On
3 (b)	-	$\overline{\text{F-01}}$	Q_5 On
4 (a)	+	$\overline{\text{F-01}}$	Q_5 Off
4 (b)	-	$\overline{\text{F-01}}$	Q_5 Off
5 (a)	+	-10 V	Q_5 On
5 (b)	-	-10 V	Q_5 On
6 (a)	+	-10 V	Q_5 Off
6 (b)	-	-10 V	Q_5 Off

Case 1 (b) Negative Input IF-01 with Q_5 On

At $e_i \approx -0.9$ V, diode D_1 forward biases, but since Q_5 is already "on," the input signal merely causes additional base current in Q_5 and drives Q_5 further into saturation. This input signal condition does not necessarily cause an "upset" unless Q_5 is damaged by excessive base current, in which case upset would occur.

Case 2 (a) Positive Input IF-01 with Q_5 Off

Since Q_5 is already "off," a positive input large enough to break down D_1 ($\approx +75$ V) and couple into the base of Q_5 will not ordinarily upset the circuit; however, an interesting extension of this case will take place if the input signal is large enough to appreciably forward bias diode D_7. If D_7 is sufficiently forward biased, a conduction path could then exist through D_5, through the collector-base diode equivalent of Q_6, through D_6 (if the drop across D_8 were sufficiently large) to the collector of Q_5, and hence to the base of Q_7 through resistor R_{B7}. Obviously, a rather large overdrive signal would be necessary in order for the above signal path to exist, but existence of such a path would cause "upset" of the Q_7 output and possibly permanent damage to D_1 and D_7.

Case 2 (b) Negative Input IF-01 with Q_5 Off

A negative input on IF-01 represents the typical mode of operation for the circuit when Q_5 is off and triggering is desired; therefore, a negative transient input on IF-01 cannot be distinguished from an ordinary input signal and "upset" will occur at $e_i \approx .9$ V when diode D_1 forward biases and causes Q_5 to change states; a situation which represents an upset condition.

Case 3 (a) Positive Input $\overline{\text{F-01}}$; Q_5 On

This case represents perhapa the most interesting "upset" condition for this circuit because of the unusual circuit path established by the input transient signal. When Q_5 is on, Q_4 will also be in the "on" state, and the nominal output at F-01 will be -0.1 volt. A positive input signal applied to $\overline{\text{F-01}}$ (the collector of Q_4) will couple through the collector-base diode of Q_4 and through R_{L6} into the collector of Q_6. Once the positive input signal affects the collector potential of Q_6, drive current through D_5 to the base of Q_5 will be inhibited and Q_5 will be cut off.

The positive signal appearing at the collector of Q_6 will also prevent normal collector current, but more important, the positive collector potential will forward bias the collector-base diode of Q_6, raise the base potential of Q_6 positively, and forward bias diode D_8 in the base circuit of Q_6. Since Q_5 is cut off, its collector potential will fall toward the negative 10-volt supply and will provide ample drive through D_6 to the base node of Q_6 to cause Q_6 to saturate under normal conditions; however, the positive potential at the base of Q_6 caused by the input transient signal will prevent any of the drive current through D_6 from affecting the operation of Q_6. Thus, the application of the positive EMP transient to the $\overline{\text{F-01}}$ terminal results in Q_5 having no base current and being cut off, and Q_6 having sufficient drive into its base node to cause saturation if the base of Q_6 were not held positive by the conduction path through D_8 and the collector-base diode of Q_6.

As the positive EMP transient at the $\overline{\text{F-01}}$ input returns toward zero, diode D_8 will first be allowed to come out of conduction (although a current path at this point will still exist through the collector-base diode of Q_6 and through D_6). Then, the base-emitter of Q_6 will receive forward drive from the D_6 - R_{C5} branch, but normal collector current will not begin because the collector of Q_6 will still be positive due to the EMP signal. As the EMP transient further approaches zero, the collector of Q_6 will be

allowed to become negative and Q_6 will go into saturation immediately since it has ample base drive through D_6 to do so. Since the collector of Q_6 will go no more negative than about -0.1 volt, the saturation value, the base drivs to Q_5, cannot be reestablishsd; thus, Q_6 will end up in the saturated state, and Q_5 will end up cut off, a condition representing a change of state for the flip-flop. Thus, an upset took place with the application of a positive input signal to the $\overline{\text{F-01}}$ terminal.

Assuming that the equivalent circuit which applies during the positive $\overline{\text{F-01}}$ input transient can be represented by the circuit shown in Figure II-8, we can predict the amplitude of input signal required to achieve upset. The R_{B4} = 10 K branch to +10 volts and the R_{C4} = 1.5 K branch to -10 vclts have been omitted since their contributions are considered negligible. The forward resistance of the collector-base diode of Q_4 is assumed to be 100 ohms.

The threshold value of E_s which will cause the potential at V_{C6} to be equal to -0.9 volt (the breakpoint of the D_5, base-emitter of Q_5 branch), will cause upset. Using the equivalent circuit of Figure II-7, the upset value of E_s calculates to be +2.285 volts. The time constant of the circuit is approximately τ = .002 μF (DPI) = (.002 μF) x (98.8) = 197.6 nsec. Since dc threshold is of interest here, there is ample time for the circuit to upset.

Case 3 (b) Negative Input $\overline{\text{F-01}}$ Q_5 On

When Q_5 is on, Q_4 is on and the logic level signal appearing at the $\overline{\text{F-01}}$ output is approximately -0.1 volt. A negative EMP transient appearing on the collector of Q_4 pulls transistor Q_4 out of saturation and forward biases diode D_4 if the transient amplitude is more negative than -3.3 volts. Damage to diode D_4 may be expsrienced if the transient amplitude and duration exceed the capabilities of D_4. If the EMP input signal appearing on the collsctor of Q_4 is more nsgative than -15 volts, collector-base breakdown of Q_4 takes place and a signal will be coupled through R_{L6} and D_5 into

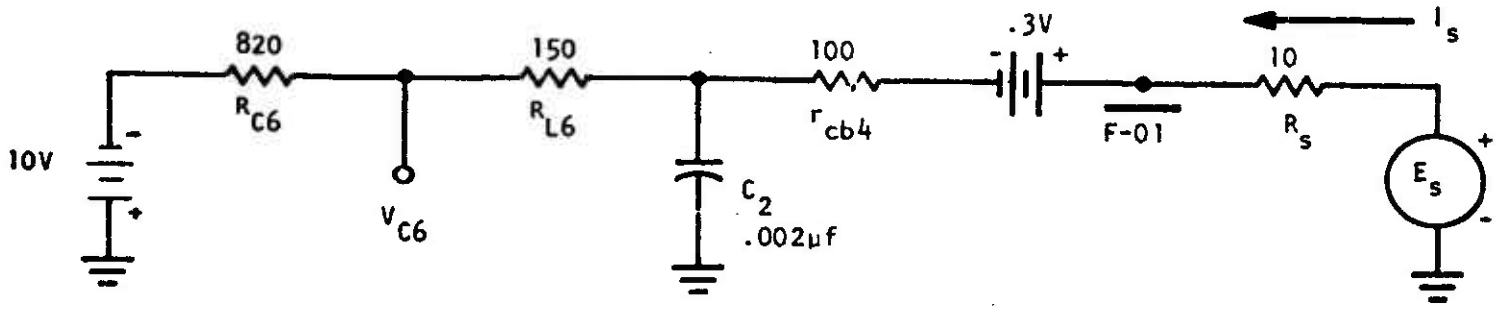


Figure II-8. Approximate Equivalent Circuit for Positive Input on $\overline{\text{F-01}}$ Terminal

the base of Q_5 but Q_5 is already on and saturated and this transient will not upset the circuit.

Case 4 (a) Positive Input $\overline{\text{F-01}}$ Q_5 Off

When Q_5 is off, Q_4 is also off and the voltage appearing at the collector of Q_4 is -3.3 volts. Since the alternate state of Q_4 is represented by an output at $\overline{\text{F-01}}$ of -0.1 volt, a positive input at $\overline{\text{F-01}}$ represents an upset condition as far as other circuits which are fed by the $\overline{\text{F-01}}$ output are concerned; however, if "upset" of the Q_5 - Q_6 flip-flop is defined as a transient input which causes Q_5 and Q_6 to change state, then the mere existence of a positive input at the $\overline{\text{F-01}}$ terminal does not necessarily represent an upset condition. The following events take place.

A positive pulse on $\overline{\text{F-01}}$ will couple through the collector-base diode equivalent of Q_4, through R_{L6} and into the collector of Q_6. At this point, transistor Q_6 will be cut off; that is, the collector voltage of Q_6 is positive, and current from the EMP transient will flow through the base-collector diode of Q_6 forward biasing diode D_8, thus, the normal base current supplied by D_6 and R_{C5} is prevented.

As the EMP transient falls back to zero, the normal base drive of Q_6 will be reestablished when $e_i \approx +.6\ V \approx (V_{CB4} + V_{CB6})$. Thus, with the reestablishment of normal base drive on Q_6, Q_6 will go back into conductions and Q_5 will again be denied base current drive and thus remain in the cutoff state.

The positive-pulse input causes many transients throughout the flip-flop, but the circuit remains in ths original state and this excitation does not causs an upset condition of the circuit (see Figure 1I-9).

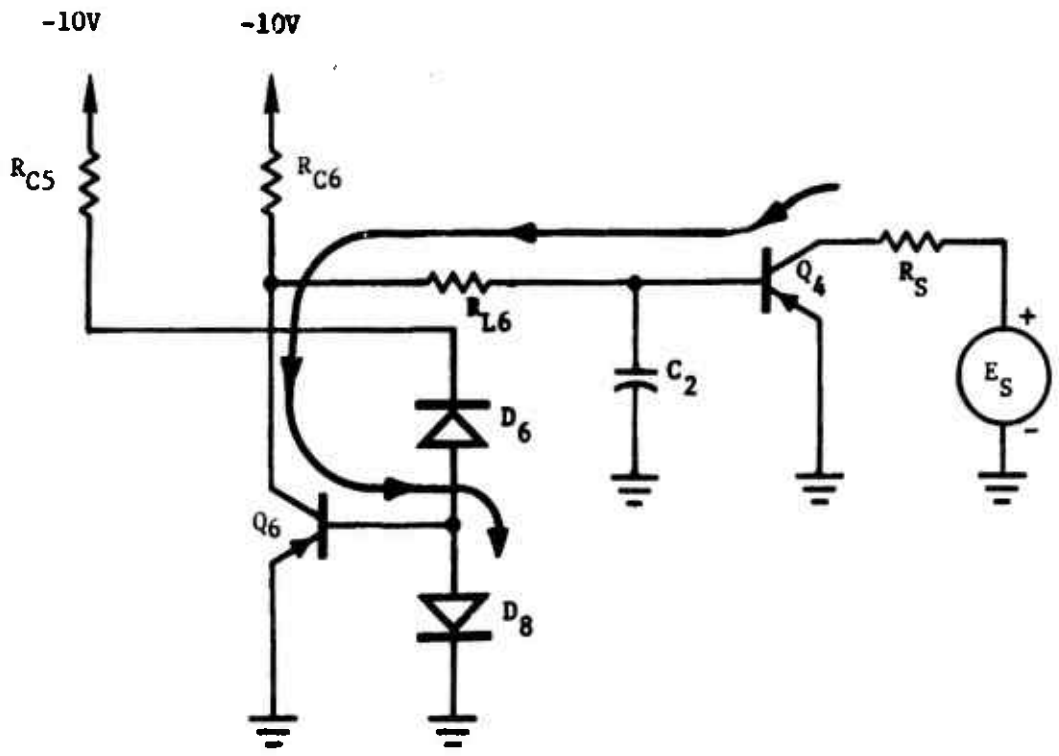


Figure II-9. Main Current Path for Case 4 (a)

Case 4 (b) Negative Input $\overline{\text{F-01}}$ Q_5 Off

Diode D_4 will try to limit output at -3.3 V, but it will not be able to accomplish this with a 10-ohm source impedance on the EMP input signal, and D_4 is likely to fail. When V_{C4} reaches -15 V, Q_4 will experience collector-base and collector-emitter reverse breakdown.

Q_4 can be made to fail and/or the signal on the base of Q_4 will couple into the collector of Q_6 and cause Q_6 to come out of saturation. The negative signal on the collector of Q_6 will cause Q_5 to come "on" and this will cause an upset condition since the flip-flop will have changed states.

Most likely, Q_4 will fail before an upset condition can occur. Such a failure will render the circuit inoperative and incapable of responding to normal logic signals.

Case 5 (a) Positive Input on -10 V Buss Q_5 "On"

Normally, a positive input signal superimposed upon the negative 10-volt buss could be used to toggle the flip-flop if commutating capacitors were employed across the cross-coupling diodes D_5 and D_6. If capacitors were employed across diodes D_5 and D_6, each would have a different charge depending on which state Q_5 and Q_6 were in. A positive pulse superimposed on the -10 V buss would cause both transistors to be cut off, and as the positive pulse terminated, the transistor whose base is connected to the capacitor of lowest charge would achieve base drive first and would come "on" and saturate. Since the transistor "off" before the pulse is applied ends up as the "on" transistor after the pulse terminates, the flip-flop toggles upon the application of each positive pulse to the -10 V buss.

Because circuit symmetry is assumed for purposes of analysis, there is insufficient diode capacitance to behave as commutating capacitors and a toggle condition is not expected to take place according to the theoretical

analysis. However, laboratory measurements performed on an actual circuit did show that the circuit would toggle from one state to the other, but it would not toggle back when the next pulse was spplied. It appeared that the circuit had a preferential state with respect to the application of a positive pulse on the -10 V power supply line. With "matched" resistors and "matched" transistors, the circuit preferred to trigger from the Q_5 "off" to the Q_5 "on" state when $\Delta e \approx +6$ volts.

When R_{C5} was reduced from 820 ohms to 730 chms, the preferential mode switched; that is, the circuit preferred to switch from Q_5 "on" to Q_5 "off," just opposite to the original preferential mode stated above.

In the original "matched" component configuration, interchanging the two transistors utilized as Q_5 and Q_6 respectively, did not alter the original preferential mode. Therefore, the preferential mode must be dependent on circuit layout and circuit components other than transistors Q_5 and Q_6.

Case 5 (b) Negative Input on -10 V Buss; Q_5 On

Regardless of the state of Q_5 and Q_6, a negative pulse superimposed on the negative 10-volt buss merely represents an increase in the supply voltage value and the "on" transistor will remain "on" and the "off" transistor will remain "off." The "on" transistor will be required to carry a larger collector current, but it will also receive a proportionally larger base drive to keep it on and saturated; therefore, no upset will occur.

Case 6 (a) Positive Input on -10 V Buss; Q_5 Off

Exactly the same argument as was given for Case 5 (a) above will apply here. The circuit will seek a preferential state, and if the circuit's

preferential state is opposite to its initial state, then an "upset" will take place. If the circuit's initial state is its preferential state, then no upset will occur.

Case 6 (b) Negative Input on -10 V Buss; Q_5 Off

See the discussion for Case 5 (b) since the same argument will apply here.

After the above hand analysis had been performed, the actual circuit was tested in the laboratory, and the expected upset conditions investigated for agreement with predictions. A comparison of the predicted and the experimental results is presented in Table II-3 and Table II-4. It is noted in Table II-3 that only those cases are presented where upset was expected; if a damage condition was expected to occur before upset took place, the test was omitted. Also, note that Case 2 (b) appears twice, once with direct coupling used and again with capacitive coupling used. In the capacitive coupling case, the input to upset should be larger than the direct coupling case by an amount aqual to the 10-volt charge on the coupling capacitor. There is good agreement in practically every case; all the "upset" conditions did occur. In Case 1 (a), the difference is in the breakdown voltage of D_1 which was approximately 75 V according to the spec sheets, but was 90 to 120 volts in reality. There is also a slight discrepancy in Case 3 (a). For some reason, the actual circuit was more sensitive than predicted, but the computer results (given elsewhere in this report) agree with the hand analysis.

In Table II-4, it is saen that predicted and measured values of tarminal voltages were in good agreement. However, the breakdown voltages of the FD-600 diodes were all greater than the spec sheets indicated.

TABLE II-3

COMPARISON OF PREDICTED AND MEASURED UPSET LEVELS

FOR DISCRETE ELEMENT FLIP FLOP

Case	Initial State	Input Terminal	Input Polarity	Pulse Width	E_i Input to Upset	
					Measured	Hand Analysis
1(a)	Q_5 "On"	IF-01	Direct Pos.	1 μsec	+ 94V	+ 75V
2(b)	Q_5 "Off"	IF-01	Direct Neg.	1 μsec	- 0.9V	- 0.9V
2(b)	Q_5 "Off"	IF-01	Capacitor (1μf) Neg.	1 μsec	- 11V	- 10.9V
3(a)	Q_5 "On"	$\overline{\text{F-01}}$	Capacitor (20μf) Pos.	1 μsec	+ 1.1V	+ 2.3V
5(a)	Q_5 "On"	- 10V Buss	Capacitor (20μf) Pos.	1 μsec	+ 5.2V	Reverts to Preferred State

TABLE II-4

COMPARISON OF MEASURED AND CALCULATED

VOLTAGES FOR DISCRETE ELEMENT FLIP-FLOP

Terminal	State	Measured	Calculated
V_{C5}	Q_5 On	- .048V	- 0.1V
	Q_5 Off	- 1.114V	- 0.9V
V_{B5}	Q_5 On	- .453V	- 0.3V
	Q_5 Off	+ .259V	+ 0.3V
V_{C6}	Q_5 On	- 1.117V	- 0.9V
	Q_5 Off	- .051V	- 0.1V
V_{B6}	Q_5 On	+ .251V	+ 0.3V
	Q_5 Off	- .451V	- 0.3V
V_{C7}	Q_5 On	- 3.350V	- 3.3V
	Q_5 Off	- .041V	- 0.1V
V_{B7}	Q_5 On	+ .105V	+ 0.0491V
	Q_5 Off	- .425V	- 0.3V
V_{C4}	Q_5 On	- .041V	- 0.1V
	Q_5 Off	- 3.347V	- 3.3V
V_{B4}	Q_5 On	- .419V	- 0.3V
	Q_5 Off	+ .102V	+ 0.0491V

Components:

R_{B7} = 9851 ohms

R_{L5} = 154.5

R_{C5} = 853.1

R_{B4} = 9861 ohms

R_{L6} = 152.6

R_{C6} = 827.2

<u>BV @ 3 ma</u>

D_1 = 96V

D_2 = 105V

D_5 = 99V

D_6 = 104V

<u>10V @ 10 Ma</u>

Q_4 β = 69.4

Q_5 β = 68.9

Q_6 β = 68.9

Q_7 β = 66.3

b. Computer Aided Analysis

The discrete component flip-flop studied in the previous section using hand analysis techniques and presented as Problem 2 was used to illustrate the applicability of various circuit analysis computer codes to the dc upset threshold prediction problem. The schematic diagram of this circuit with nodes identified for formatting is shown in Figure II-10.

While many computer codes capable of solving dc upset threshold problems are available, only CIRCUS-2, NET-2, and SCEPTRE (References 8, 9, and 10) were used for purposes of demonstration. In each case, the latest edition of the code user's manual was used to format flip-flop circuit.

For any given circuit upset problem, the following problems relating to the use of computer codes must be considered.

(1) The applicability of active device models to the problem being addressed.

(2) The extent of the device library associated with the code selected or available.

(3) Special considerations that require attention during the formatting procedure.

As stated in Appendix A, most circuit analysis codes use either some modification of the Ebers-Moll Model or a charge control equivalent. For dc or low frequency (< 20 MHz) transient circuit upset problems, the models generally available are adequate. The problem most frequently encountered is that of a limited device library. If a given device is not available in the library, one must select a suitable equivalent,

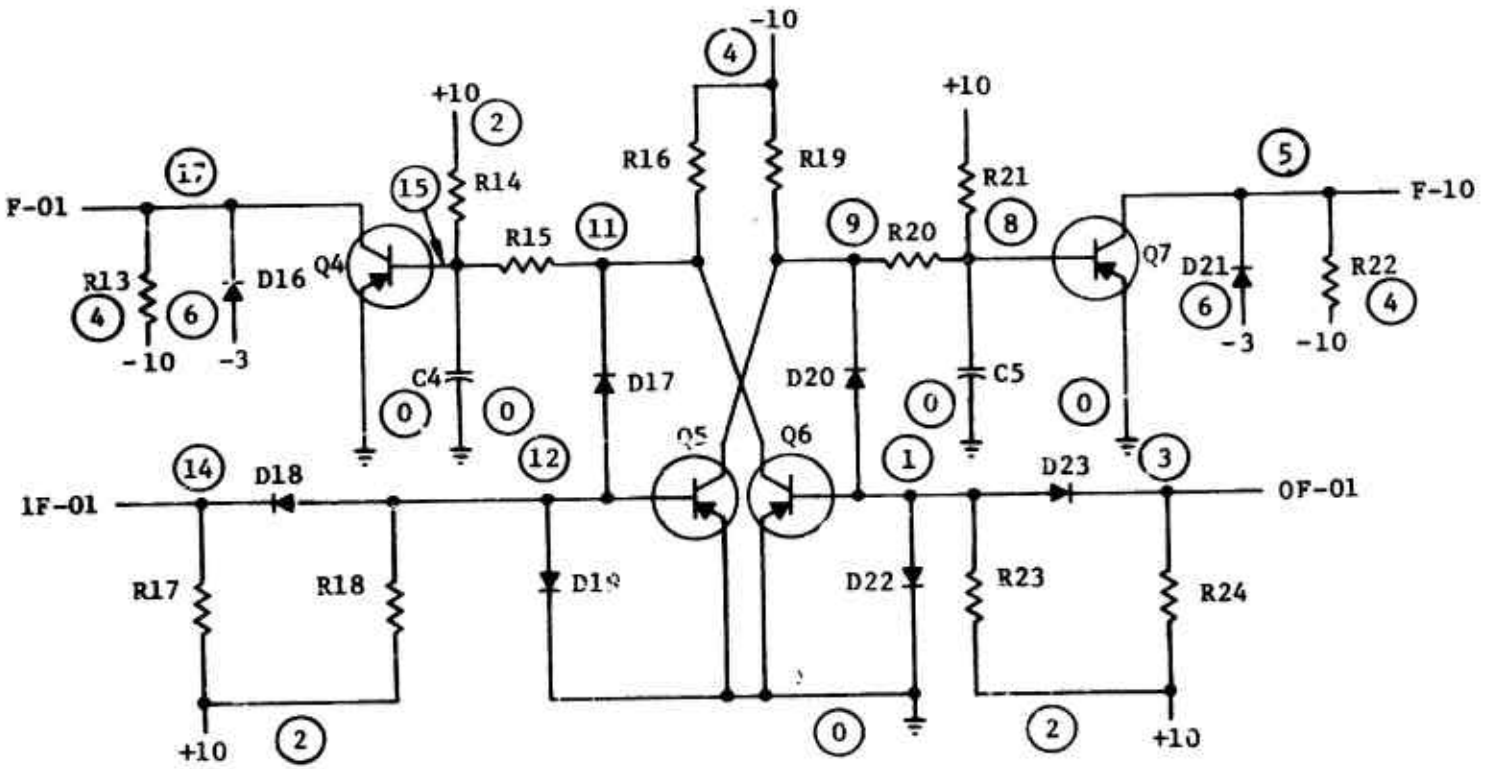


Figure II-10. Discrete Component Flip-Flop Showing Node Numbering for Computer Coding

determine required device parameters, or obtain device data from another library and modify the available parameters. Of the three codes used, SCEPTRE was found to have the most complete and accurate device library.

The special considerations referred to by Item (3) above include such problems as deriving realistic initial conditions and modifying schematic values to recreate circuit asymmetry such as exists in flip-flops. The evaluation of these factors requires some degree of hand analysis in order to prepare a computer input.

Computer runs were made for each of the cases where upset was predicted by hand analysis. A 1 μsec pulse duration was used in all cases. For the initial run, the input voltage pulse amplitude was set to a level below the predicted dc upset level and then increased with each succeeding run until upset occurred. The initial state of the flip-flop was set in one of two ways. For the SCEPTRE and NET-2 programs, a current generator delivered a short current pulse to one of the inputs prior to the start of the upset pulse. There was a delay of 300 nsec between the current pulse and the upset pulse to allow the circuit time to stabilize before the upset pulse was applied. The initial conditions for the CIRCUS-2 runs were calculated by the program after initial estimates were given. Table II-5 shows a comparison of the various upset cases for experimentally determined values, hand analysis predictions, SCEPTRE, NET-2, and CIRCUS-2 predictions. The differences seen in Case 1 (a) are due to the different assumed values for the breakdown voltage of diode D_1. The differences seen in Case 3 (a) are due to differences in the model parameters of the transistors and diodes. In Case 5 (a), the flip-flop was not in its preferred state and therefore an upset was measured. This is one of the cases where the computer analyses, because of the symmetry of the circuit, cannot predict the upset unless a preferred state is programmed.

As an illustration of the effect that the semiconductor model will have in predicting upset, the discrete flip-flop circuit was analyzed using a 50 nsec pulse. For this shorter pulse width, the upset threshold predicted by the

TABLE II-5 SUMMARY OF UPSET ANALYSIS RESULTS

Case Number	Initial State	Input Terminsl	Input Polarity	Input Coupling	Pulse Width	INPUT REQUIRED FOR UPSET				
						MEASURED	HAND ANALYSIS	COMPUTER ANALYSIS		
								SCEPTRE	NET-2	CIRCUS
	Q5 "on"	IF-01	POSITIVE	DIRECT	1 µsec	+94V	+75V	+100V	+100V	+90V
1(a)	Q5 "on"	IF-01	POSITIVE	DIRECT	500 ns	+94V				
	Q5 "on"	IF-01	POSITIVE	DIRECT	100 ns	+94V				
	Q5 "off"	IF-01	NEGATIVE	DIRECT	1 µsec	-0.90V	-0.90V	-0.90V	-0.90V	-1.0V
2(b)	Q5 "off"	IF-01	NECATIVE	DIRECT	500 ns	-0.95V				
	Q5 "off"	IF-01	NEGATIVE	DIRECT	100 ns	-1.15V				
	Q5 "off"	IF-01	NEGATIVE	20 uf	1 µsec	-11.0V	-10.9V	-11.0V	-11.0V	-11.0V
2(b)	Q5 "off"	IF-01	NEGATIVE	20 uf	500 ns	-11.0V				
	Q5 "off"	IF-01	NEGATIVE	20 uf	100 ns	-11.5V				
	Q5 "on"	F-01	POSITIVE	20 uf	1 µsec	+1.1V	+2.3V	+2.3V	+2.1V	+3.0V
3(a)	Q5 "on"	F-01	POSITIVE	20 uf	500 ns	+1.15V				
	Q5 "on"	F-01	POSITIVE	20 uf	100 ns	+1.9V				
	Q5 "on"	-10V BUS	POSITIVE	20 uf	1 µsec	+5.2V	NO PREDICTION	NO UPSET	NO UPSET	NO UPSET
5(a)	Q5 "on"	-10V BUS	POSITIVE	20 uf	500 ns	+18.0V				
	Q5 "on"	-10V BUS	POSITIVE	20 uf	100 ns	+28.5V				
	Q5 "on"	-10V BUS	NEGATIVE	20 uf	1 µsec	NO UPSET	NO PREDICTION	NO UPSET	NO UPSET	NO UPSET
5(b)	Q5 "on"	-10V BUS	NEGATIVE	20 uf	500 ns	---				
	Q5 "on"	-10V BUS	NEGATIVE	20 uf	100 ns	---				

NOTE: Data are presented only for cases where upset was predicted by Hand Analysis.

three different analysis programs agree as well as with the longer (1 μs) pulse. These differences can be seen in Figure II-11 which shows the input voltage (IF-01) required to upset the flip-flop for the three analysis programs. The primary difference in the results is probably due to differences in the device capacitance values used in the different codes. As pointed out previously, conservative results are obtained using dc upset threshold in conjunction with a high frequency approximation such as the one derived earlier in this section. Using the expression

$$V_u = V_{dc}\left(\frac{t_{pd}}{t_u}\right)^{1/2}$$

with the known values of $V_{dc} = 0.9V$ and $t_{pd} = 200$ ns, the upset threshold for a 50 ns pulse is

$$V_u = 0.9\left(\frac{200}{50}\right)^{1/2} = 1.8 \text{ volts}$$

This value is in the range predicted by the computer analysis and is an acceptable approximation.

6. REFERENCES

The following references were used in this chapter.

1. Gray, R. M. (1971), "An Experimental Investigation of EMP Induced Transient Upset of Integrated Circuits," Sandia Laboratories Report SC-TM-71-0330, June 1971.

2. Lange, T. J. (1971), "In-Place EMP Wing III Threshold Variation Study," Boeing Document D2-19693-3, August 1971.

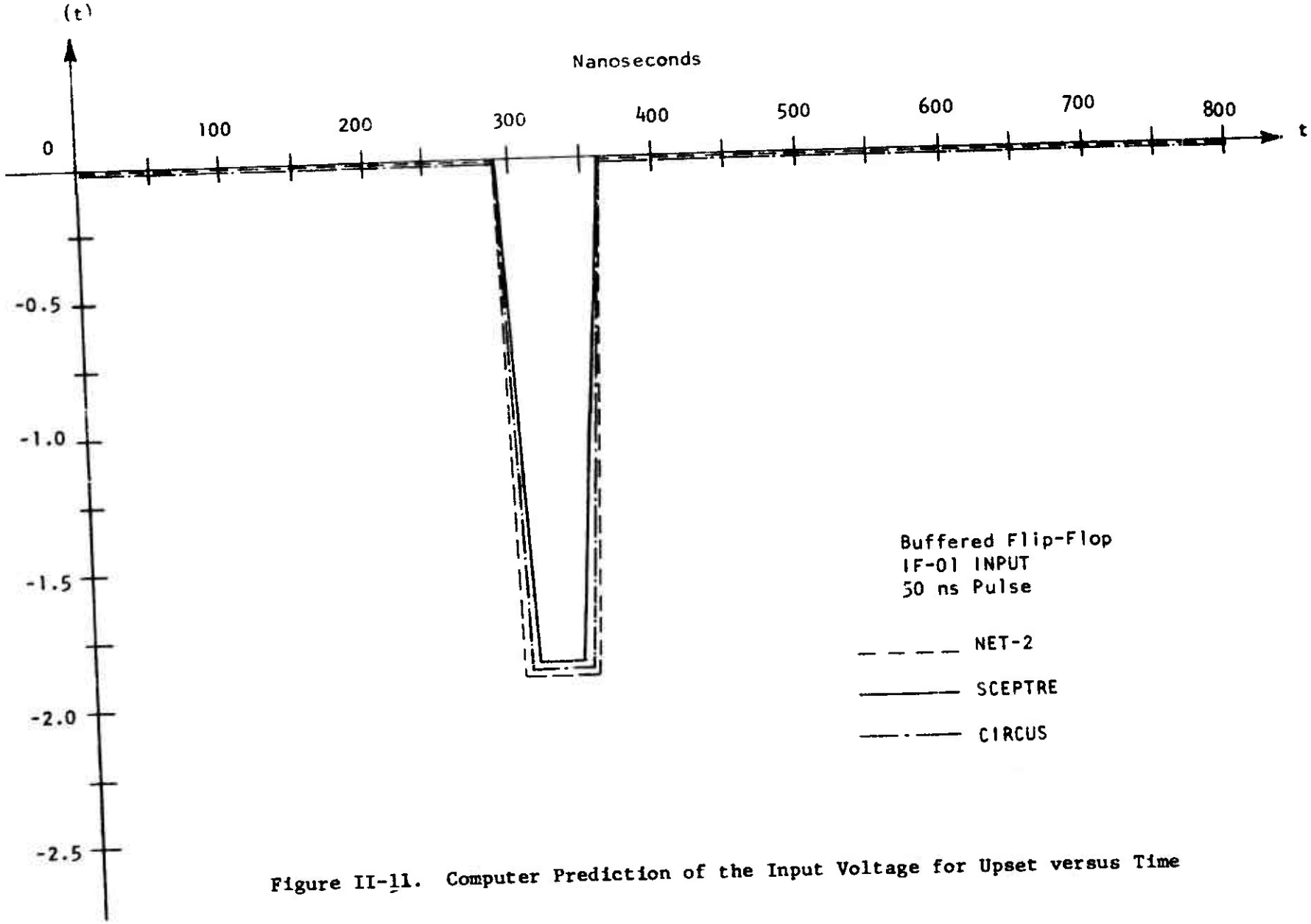


Figure II-11. Computer Prediction of the Input Voltage for Upset versus Time

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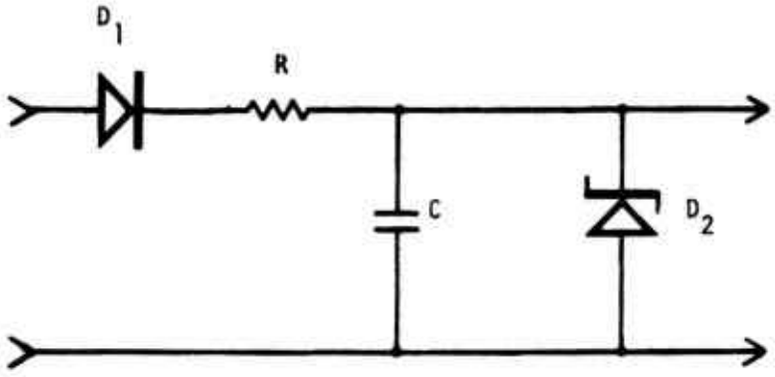
SECTION III

DAMAGE THRESHOLD ANALYSIS

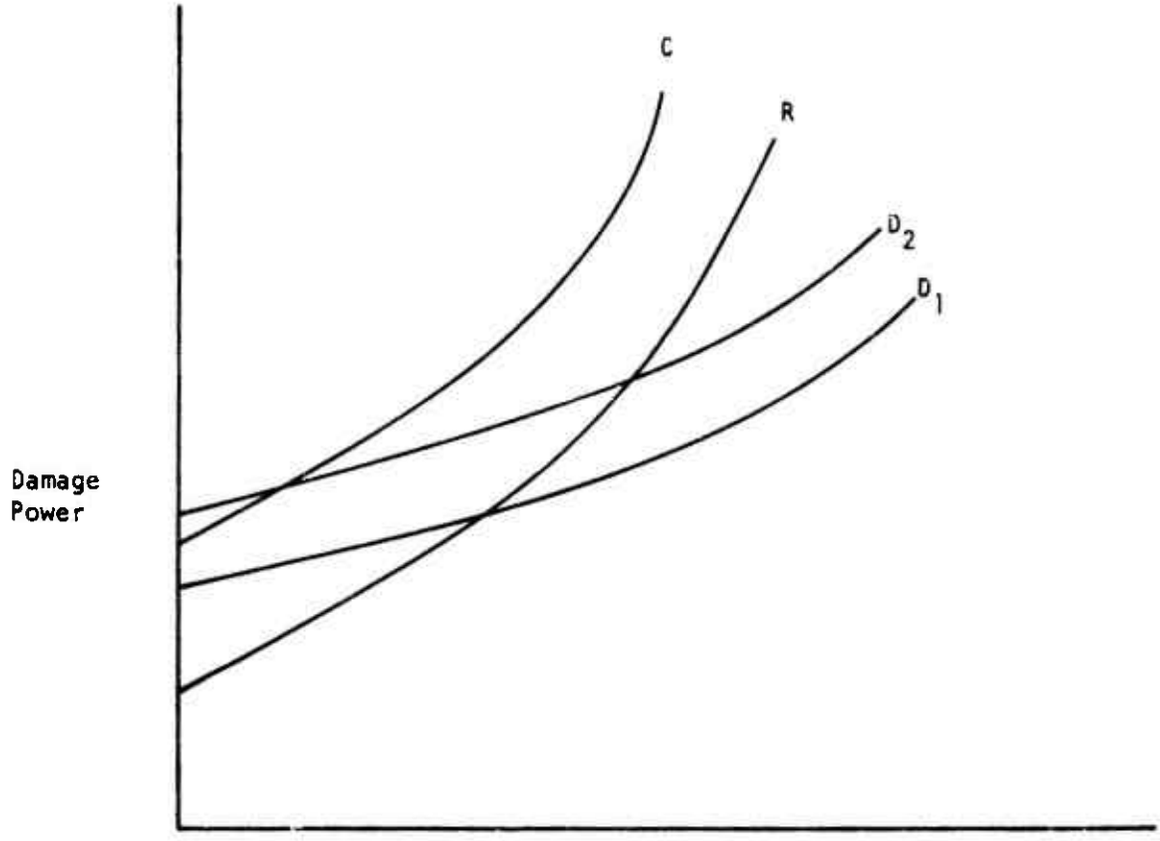
1. GENERAL

Component burnout or permanent damage has been previously defined as the irreversible degradation of a component's characteristics due to an EMP induced transient. Damage threshold analysis refers to the circuit level analysis performed to determine the magnitude of the smallest signal, of a specified time history, that will cause the pulse power burnout of the most susceptible component associated with a given circuit port. This component damage level is a function of frequency, therefore the pulse power necessary to cause permanent damage must be computed for all frequencies of interest. Figure III-1 illustrates a hypothetical damage threshold assessment problem. Figure III-1a is a simplified schematic of an interface circuit selected using a circuit screening procedure as described in Section I. The damage characteristics of each component are shown in Figure III-1b. The actual damage threshold curve for active devices is dependent on transient polarity; therefore, Figure III-1b would apply only to one input polarity. To determine circuit vulnerability, the analyst computes actual device power dissipation for the given EMP specification and compares the actual level with the rated damage level.

It is obvious from the above statements that the performance of a thorough damage threshold analysis requires a data base that permits the complete characterization of the pulse power response of all generic component types. Since component exposure to high amplitude, short



(a) Interface Circuit Schematic



(b) Component Damage Power Profiles

Figure III-1. Hypothetical Damage Threshold Assessment Example

duration, EMP induced transients often results in a nonlinear response not defined by existing device models, each generic component class (resistors, capacitors, junction semiconductors, etc.) must be studied sepsrately in order to develop models and, subsequently, a complete data base for damage threshold analysis.

Based on device population in modern aeronautical systems and on limited experimental work by several investigators (References 1 through 7), most damage threshold analyses assume that the semiconductor junction is particularly susceptible to damage for the frequencies or pulse widths of interest. Based on this assumption, most component level transient response studies have centered around semiconductor junction devices. Since the available pulse power response data base is limited primsrily to transistors and diodes, the analyses presented in this handbook will emphasize the calculation of damage thresholds determined by semiconductor device types. Cases where other device types could determine the damage threshold of a given circuit port will be pointed out when encountered in sample problems.

A number of investigators are currently performing pulse testing programs to study the damage levels and mechanisms for integrated circuits and resistors. Ultimately the data obtained from these programs, along with data obtained from previous similar programs, will be stored in the data storage/retrieval computer code, SUPERSAP (Reference 8).

Once a circuit has been selected for s detailed damage threshold anslysis (by a screen as discussed in Section I), the computation of damage thresholds will proceed as follows:

(1) Select evaluation method

   (a) Hand analysis
   (b) Computer analysis
   (c) Experimental assessment

(2) Obtain circuit data (i.e., component values, active device parameters, operating levels, etc.)

(3) Examine each circuit node for possible intereat

(4) Perform threshold analysis for each interface port

   (a) Simplify the circuit using network analysis techniques.
   (b) Select or compute damage power as a function of frequency [P(f)] for each component in the simplified circuit.
   (c) Compute circuit port V-I required to generate the lowest P(f) determined in (b).
   (d) Compare component dissipations due to input (c) with each damage level to verify that the lowest P(f) selected is the worst case.
   (e) If the loweat component P(f) is not the worst caae, recompute circuit port V-I for the moat susceptible component.

(f) Evaluate circuit layout and packaging for possible arcing modes.

(g) If circuit vulnerability is to be assessed, determine the applicable driving function and source impedance (Section IV). Vulnerability is determined by comparing the actual driving function to the results of (e).

(h) Enter data into susceptibility matrix or computer data base.

For the purposes of this handbook, it is assumed that only interface circuit ports need be considered. This assumption is generally true for the damage case due to the low probability of delivering large powers by other than direct coupling. Nevertheless, the circuit layout and packaging should be studied for possible arcing modes.

The circuit element having the lowest damage threshold [P(f)] at a given frequency does not necessarily determine the lowest "circuit" damage threshold. As indicated by the inclusion of threshold analysis steps 4(d) and 4(e), the computation of worst case (lowest) circuit port V-I may be an iterative process. The number of iterations will depend on the circuit configuration and hence power distribution. For example, in Figure III-1, the power dissipation in resistor R (I^2R) may exceed that component's damage rating at a current, I, less than that required to fail diode D1, even though the damage threshold for D1 is less than that for R. Hence in this case the resistor may be the most susceptible circuit element. Such a case is encountered in example problem 2 in Section 5.a.

This procedure assumes a complete component damage threshold data base so that all components can be given consideration. In actuality the existing data base is limited to junction semiconductor devices and contemporary damage threshold analyses assume that these components

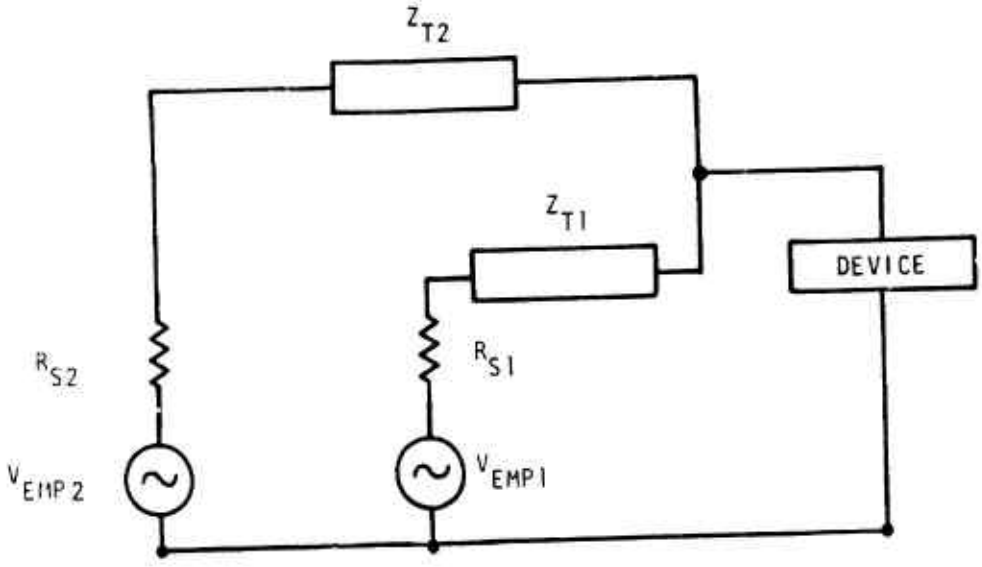
determine circuit susceptibility levels. As pointed out, this assumption will not be accurate in some cases and the analyst should utilize the generalized procedure in conjunction with the data base available at the time the analysis is performed.

As in the case of transient circuit upset, any circuit node exposed to an EMP induced transient must be analyzed to determine its damage threshold level. In the general case, a circuit selected for analysis will contain several exposed ports and each must be analyzed separately and in combination with other ports to completely characterize the circuit's EMP damage susceptibility.

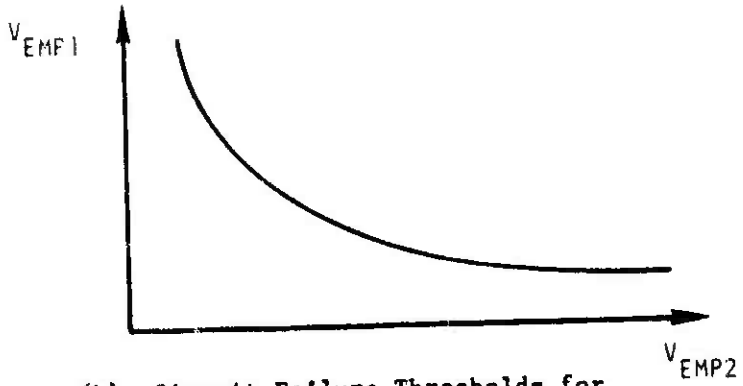
Assuming that a particular device has been identified as the most susceptible element associated with a given circuit node, Figure III-2 illustrates a two port excitation case. The effect of each transient source on the device may be represented by a transfer impedance designated by Z_T, which is the ratio of the change of signal voltage of the source to the change of device current. The pulse power dissipated in the device is a function of both EMP signal sources, their transfer impedances, and the phase relationship of the pulses.

Unless definite amplitude and phasing characteristics for the signal sources can be determined, there will be an infinite number of combinations of phases and/or amplitudes which can cause the device to fail. This may occur even if one of the parameters (amplitude, for instance) is variable while the other (phase) is kept fixed. For this case, the voltage threshold at the circuit necessary to fail the device may be represented graphically in a manner similar to Figure III-2b. Any point on the graph would define a combination of defined phase signal sources required to fail the device.

If a relationship for both the phase and amplitude of the two EMP sources can be defined, then one combination of EMP source voltages will



(a) Equivalent Circuit of a Two Port Excitation Case



(b) Circuit Failure Thresholds for Two Port Case

Figure III-2. Two Port Excitation Example

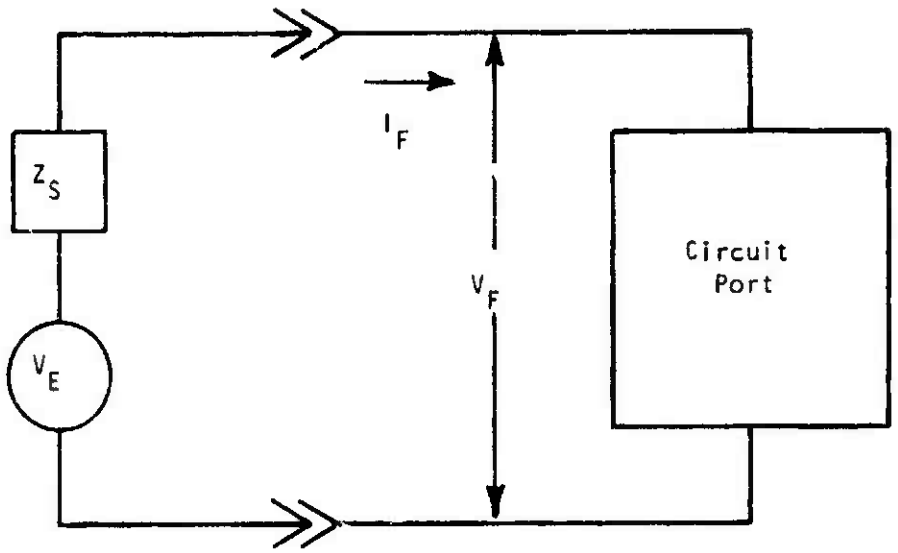
define the circuit failure thresholds. It can be seen from the above discussion that the analysis of multiport EMP damage for a case where the exact sources are not known, is a complicated process. For the case where every EMP source is completely specified and invariant, a definite multiport failure level may be determined for the circuit. However, it may still be desirable to generate a curve such as Figure III-2b to determine the margin of safety or overkill for the circuit. Fortunately, in most cases, one of the transfer impedances will dominate (i.e., be significantly smaller than the rest). For this case, the multiport nature of the circuit excitation may be ignored and the analysis may be conducted considering only the EMP source acting through this dominant impedance. The determination of the relative magnitudes of the transfer impedance may be made by inspection for simple circuits. For more complicated circuits, circuit analysis techniques such as the Driving Point Impedance (DPI) method (Appendix C) may be used.

2. RESPONSE CONSIDERATIONS

Damage threshold analyses can be performed in one of three ways:

(1) Given a specific interface circuit, determine the component damage threshold ratings for all components and from these expressions, compute the smallest input signal, of a specific waveform, that will produce permanent damage. This is the most general form of solution and is independent of driving function and source impedance. Referring to Figure III-3, V_F and I_F as a function of frequency are determined.

(2) Given a worst case (amplitude and waveform), EMP excitation determine the minimum vulnerability threshold. In this case, component and circuit damage thresholds are computed only for the actual worst case driving function (V_E) and source impedance given (Z_s). Referring to Figure III-3, a worst case value for Z_s is defined and the associated V_E is computed as



V_F - Minimum Failure Voltage

I_F - Minimum Failure Current

Z_S - Source Impedance

V_E - EMP Generator Voltage

Figure III-3. EMP Excitation Variables

$$V_E = V_F + I_F Z_s$$

In general this approach is used in the absence of a verified EMP specification to estimate the relative vulnerability of many circuit ports in a given subsystem.

(3) Given a specific EMP specification (based on either theoretical or experimental data), use the data from (1) in conjunction with the known source impedance to determine minimum vulnerability threshold and then compare this value with actual source voltage for all frequencies of interest. In this case, both V_E and Z_s (Figure III-3) are known and vulnerability can be more accurately assessed than for (2). Therefore

$$V_E(\text{threshold}) = V_F + I_F Z_s$$

$$\frac{V_E(\text{actual})}{V_E(\text{threshold})} \longrightarrow \text{Vulnerability}$$

The particular approach used depends entirely on the objective of the analysis and the information available. Giving complete damage characterization for all components and an EMP specification, method (3) is used.

Since the example problems presented later in this section are intended to illustrate a general approach, method (2) is used with various resistive source impedances. Large magnitude current pulses are required

to produce permanent damage, hence the value of source impedance is extremely important in determining if circuit damage will occur for a given generator voltage. The failure threshold of a circuit for a single input drive is the lowest input current (I_F) which will cause a failure current to flow in a critical circuit component. As this input current must also flow through the source impedance, a proportionally higher generator voltage will be required as the source impedance magnitude is increased. The source impedance in a damage analysis places an upper limit on the amount of current that can be drawn from the source at a given voltage. As will be shown later by sample Problem 4, the value of source impedance selected can possibly determine the failure mode exhibited by a given circuit.

Since the EMP specifications are often stated in terms of a damped sine wave and since most component failure data are defined in terms of a rectangular pulse, a relationship between these two waveforms is often required. For the junction devices, a detailed derivation of such a relationship is presented in Appendix B. Given a damped sine wave of specified frequency, a rectangular pulse producing identical junction degradation may be defined using the following equation:

$$\tau_P = \frac{1}{5f_s}$$

where

τ_P = duration of rectangular pulse

f_s = frequency of damped sinusoid

As shown in Appendix B, this relationship gives a good approximation for either the forward or reverse bias cases. Based on multiple pulse studies by Wunsch and others (References 2 and 7), it is assumed that device damage will occur during the first cycle of a damped sine wave, if

at all. Therefore, the lower amplitude cycles are neglected. Waveform conversion expressions for other component types have not been derived at this time.

3. ANALYSIS METHOD SELECTION

The general discussion of the relative merits of hand analysis, computer aided analysis, and experimental assessment presented in the upset threshold analysis section also applies to damage threshold analysis with the following additionsl factors:

(1) The limited component damsge characteristic dats base necessitates the use of experimental assessment for many circuit cases. At the present time, insufficient information is available to permit the theoretical determination of integrated circuit damsge thresholds.

(2) Exposure to high amplitude transients force most component types to operate in abnormal modes; thus, conventional small and large signal device models are not generally valid. Special damage models such as junction breskdown models hsve not been incorporated in most available transient analysis computer codes.

(3) The use of simple device breakdown models in conjunction with circuit simplification techniques, such as DPI and loop anslysis, permit hand analysis to solve even complex circuits; thus making this method preferable.

Figure III-4 ia the analysis technique selection matrix for damage problems. The weighting of individual selection factors for each snalysis

DISCRETE CIRCUITS							
SELECTION FACTORS / TYPES OF ANALYSIS	CIRCUIT COMPLEXITY	PROBLEM COMPLEXITY	DATA REQUIRED	ACCURACY REQUIRED	ECONOMY	NUMBER OF SIMILAR ANALYSES	TOTAL
HAND	1	3	2	-	1	1	8
COMPUTER	2	2	3	-	3	2	12
EXPERIMENTAL	3	1	1	-	2	3	10

Figure III-4. Damage Threshold Analysis Technique Selection Matrix

technique is ordered such that the lowest numerical rating indicates highest preference. While each analysis method has its advantages and limitations, hand analysis has been found to be the most effective overall approach. Experimental determination of damage thresholds requires more sophisticated laboratory facilities than upset analysis because of the high power, high frequency signals that must be generated to produce device failures. At the present time, few computer codes are available that contain device burnout models. Even if existing codes are modified to include this feature, existing burnout models are not precise and hand analysis is acceptably accurate and generally more cost effective. Circuits containing input filters or a large population of reactive components may best be solved using computer techniques. As damage models are improved and required device libraries, such as SUPERSAP, are developed, the use of computer codes for damage threshold analysis may become more practical and cost effective. The optimum analysis approach at the present time is hand analysis supplemented by experimental work when no device model is available.

4. DATA REQUIRED FOR DAMAGE ANALYSIS

The most important data required for a damage analysis are the damage threshold charactistics [P(f)] for all the components in the circuit under study. As stated earlier in this section, semiconductor devices are considered most susceptible to pulse power burnout and are generally assumed to be the single most critical item in any circuit. Therefore, most work done to date regarding component transient response has involved discrete junction semiconductor devices. In order to perform damage threshold analyses, the pulse power damage characteristics of a wide range of semiconductor devices must be known. The development of models that will predict the failure levels of junction semiconductor devices and the generation of a data base have been pursued by several investigators (References 1 through 7). For the frequency range, hence pulse

width range, or primary interest, the Wunsch model (Reference 1) is widely used. This model relates the pulse power required to produce junction burnout to the pulse width. This model has the form of:

$$P_j = K_R t^{-1/2}$$

where P_j is pulse power required to produce junction failure, t is pulse duration, and K_R is a device constant dependent on such factors as junction geometry and material. This equation states that the pulse power required to cause localized melting in a semiconductor junction is a function of the pulse width (or frequency) of the incident signal. This model was developed and experimentally evaluated for the reverse bias case and for pulse widths in the 50 nanosecond to 20 nanosecond range. Applying the model, the current to produce junction failure (I_j) is

$$I_j = \frac{P_j}{V_{BD}} = \frac{K_R t^{-1/2}}{V_{BD}}$$

where V_{BD} is the junction breakdown voltage in the reverse bias direction. This expression neglects bulk resistance (R_B) heating effects since the basic thermal model for junction failure assumes that dissipation in the bulk material is negligible. Therefore, the "device" power (P_D) to produce failure may be expressed as

$$P_D = I_j V_D = P_j + P_B$$

where

V_D = Voltage across the device

P_B = Power dissipated in the bulk material

or

$$P_D = I_j V_{BD} + I_j^2 R_B$$

Although device power, P_D, is not generally equal to junction power, P_j, this equality is often assumed correct to allow simple experimental determination of damage constant, K, using the Wunsch model

$$K_{R_1} = P_D t^{1/2}$$

or

$$K_{R_1} = (V_D I_j) t^{1/2}$$

This technique will be in error due to the inclusion of power dissipated in the bulk resistance, but is sufficiently accurate for the determination of relative damage characteristics of a wide range of semiconductor device types. Since

$$P_D > P_j$$

a more conservative (lower) K would be determined using the relationship

$$K_{R_2} = P_j t^{1/2}$$

or

$$K_{R_2} = (V_{BD} I_j)\ t^{1/2}$$

K_{R_1} and K_{R_2} have been assumed equal and have therefore been used interchangeably. For the purpose of this handbook the bulk resistance heating is assumed independent of junction heating and the basic Wunsch equation will be used to determine the current required to fail a given junction. Bulk resistance will be treated as an independent element which must be known to assess the total circuit input power required to cause failure.

While the damage constant, K_{R_1}, can be obtained experimentally by pulse testing, a theoretical method for the computation of K using manufacturer's specifications has also been developed (Reference 4) and is a less costly although less accurate technique. The following two general approaches have been formulated to determine K:

(1) Junction Capacitance/Breakdown Voltage Method.

(2) Thermal Resistance Method.

Figure III-5 is a summary of the theoretical methods available for computing semiconductor damage constants. Method (1) above is more accurate and the parameters required can be readily measured or obtained from manufacturer's specifications.

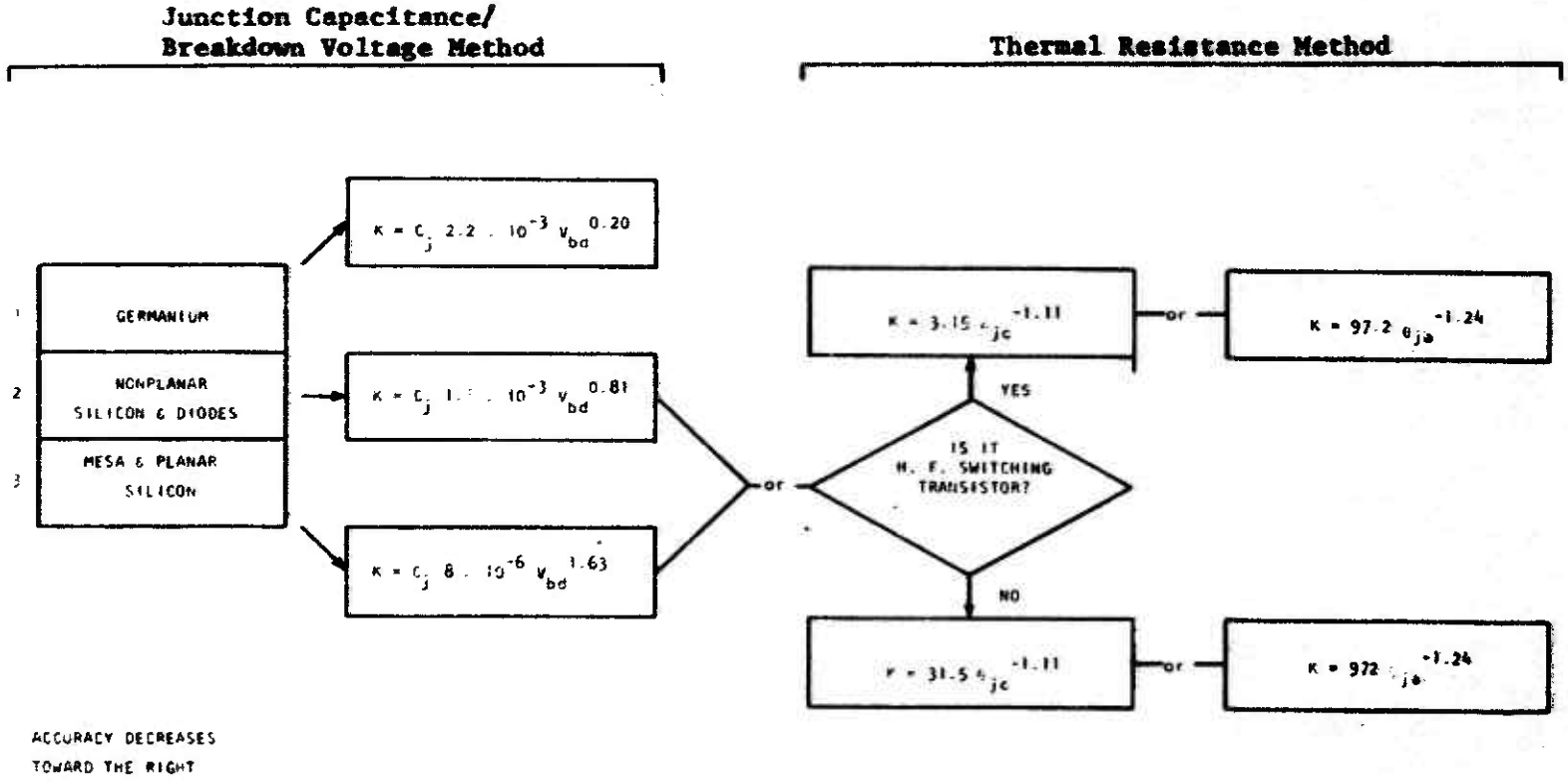


Figure III-5. Summary of Methods Available for Computing Damage Constants

Figures III-6 through III-8 present nomographs for quick determination of damage constant using the junction capacitance/breakdown voltage method. The source of the voltages and capacitances used in this method have considerable impact on accuracy. Manufacturers usually specify only minimum (V_{BD}) and maximum (C_j) values and the measured values for a specific device may differ from the specification value by more than an order of magnitude. A listing of some measured and calculated semiconductor device damage constants and breakdown voltages is presented in Appendix D. The Air Force Weapons Laboratory has designed a computer code, SUPERSAP (Reference 8), which permits the retrieval of known semiconductor device transient response data. This code has recently become operational and will be a good source of device EMP response data.

Semiconductor junction damage studies performed by Wunsch and others have shown that less power is required to produce junction failure in the reverse bias direction (K_R) than in the forward bias direction and that, for transistors, the damage constant for the emitter-base junction (K_{e-b}) is lower than that for the collector-base junction (K_{c-b}). Considering the inequalities shown below, plus the limited testing done for other than the reverse bias junction case, one can see that the data base for junction devices is incomplete. The question marks in two of the inequalities indicate that a relationship has not been defined at this time.

$$K_R < K_F$$

$$K_{e-b_R} < K_{c-b_R}$$

$$K_{e-b_F} \; ? \; K_{c-b_F}$$

$$K_{c-b_F} \; ? \; K_{e-b_R}$$

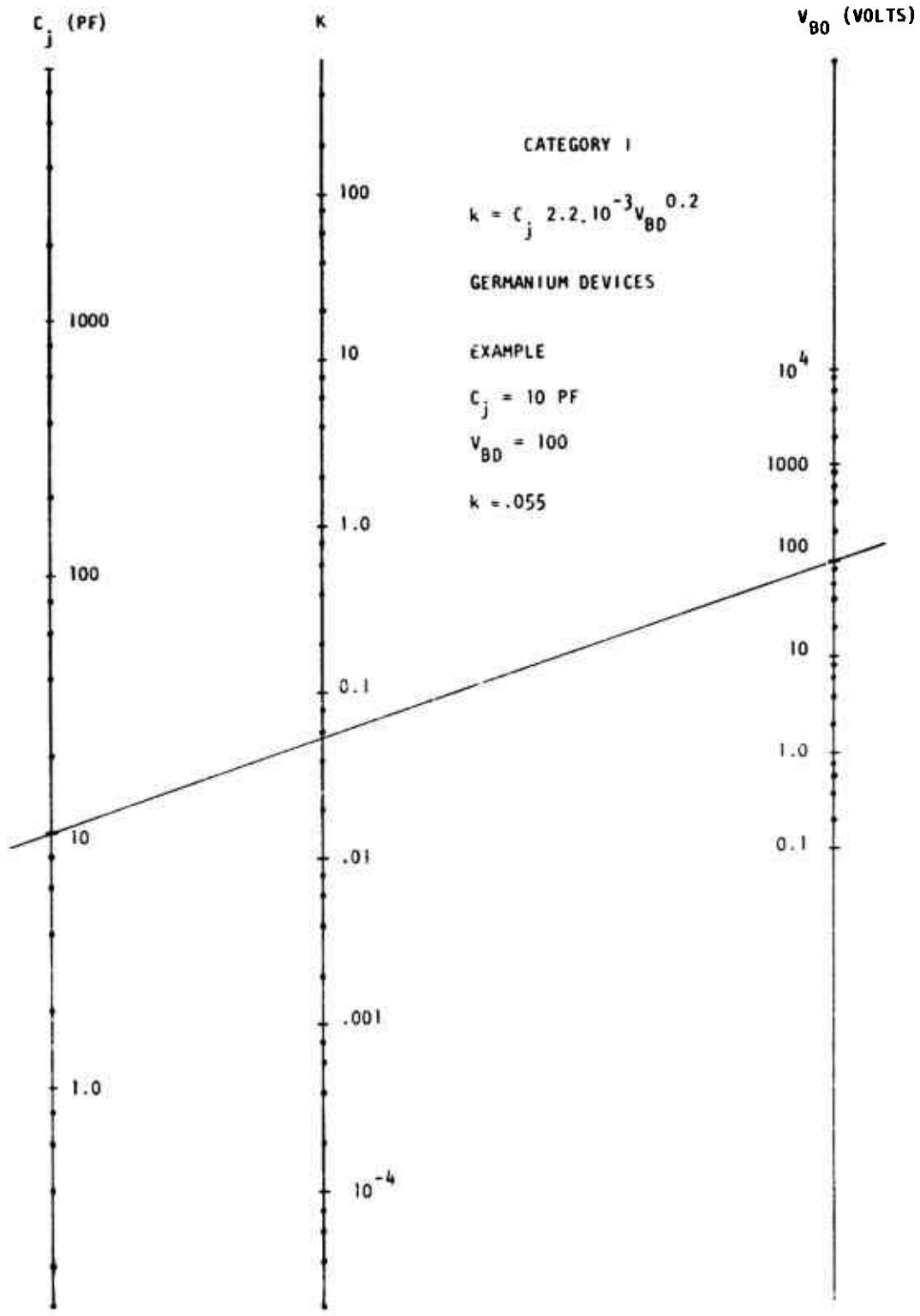


Figure III-6. Nomograph to Determine Damage Constant for Germanium Devices

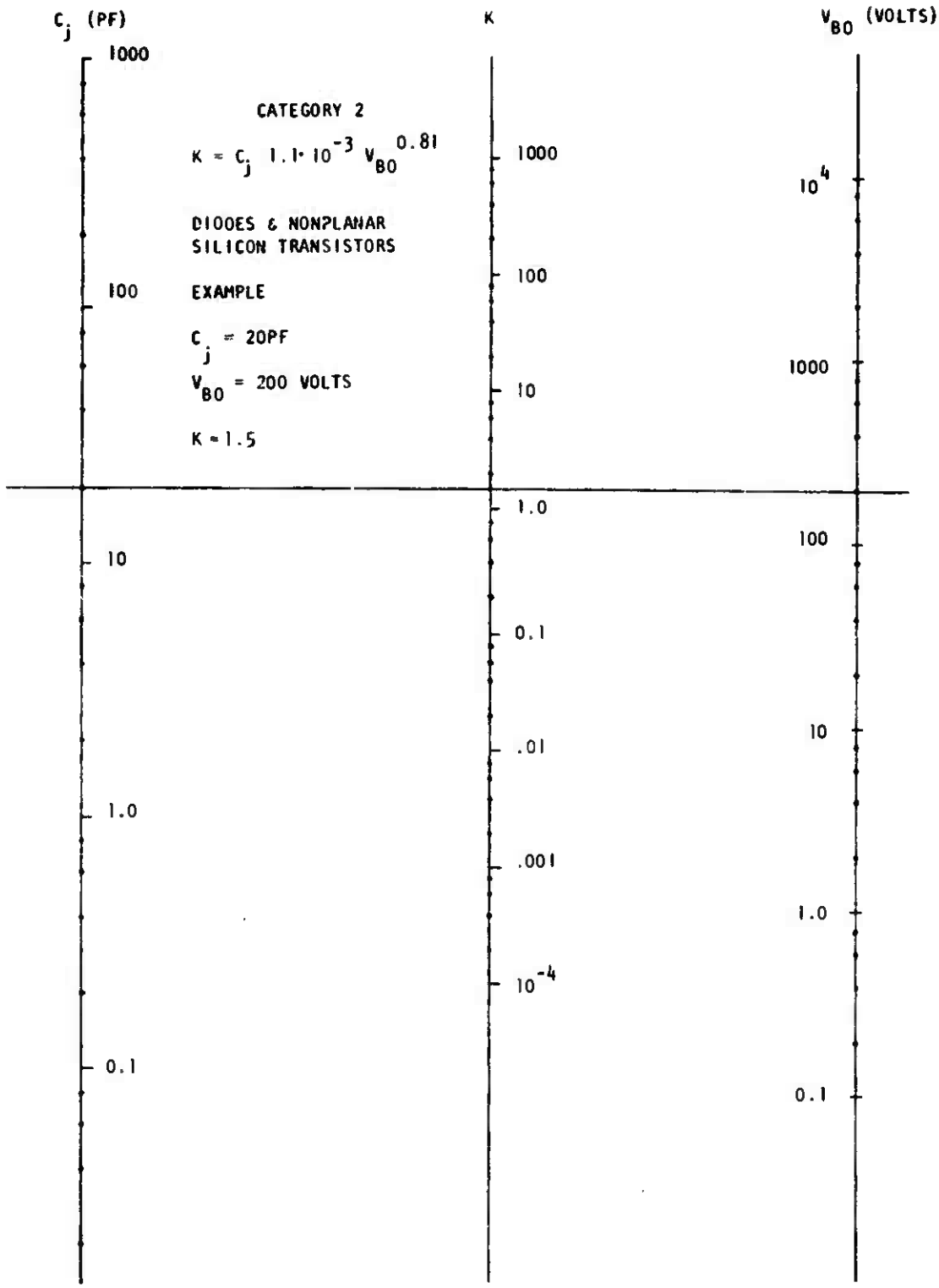


Figure III-7. Nomograph to Determine the Damsge Constant for Diodes and Nonplanar Silicon Transistors

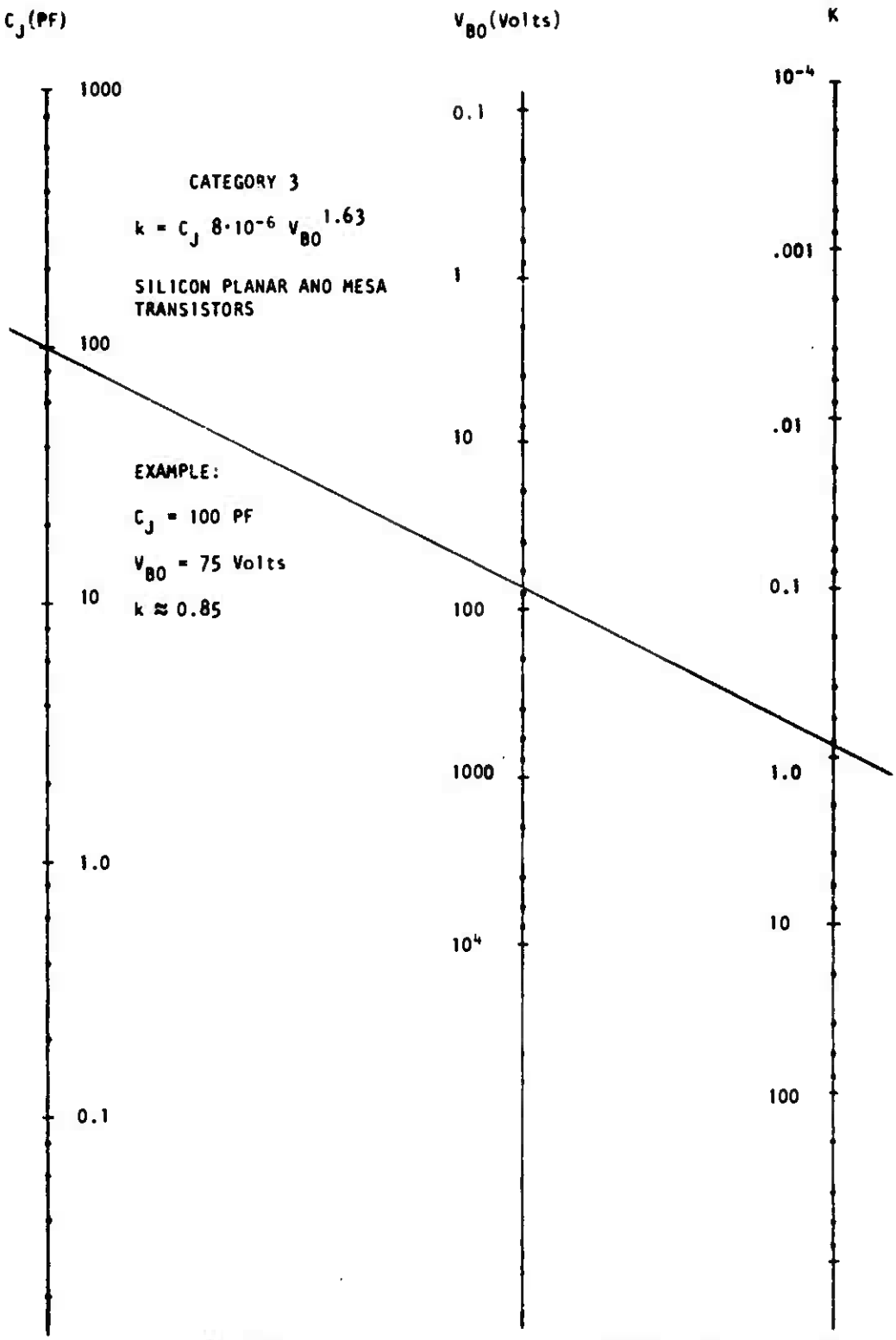


Figure III-8. Nomograph to Determine the Damage Constant for Silicon Planar and Mesa Transistors

It is known that junction failure in the forward bias case is primarily caused by heating in the bulk material. The power to produce junction failure under forward bias (P_F) conditions has been theoretically approximated as

$$P_F = K_F t^{-1}$$

but experimental work has shown the $t^{-1/2}$ time dependency of the basic Wunsch equation to be reasonably accurate. No theoretical method is available for computing the forward bias damage constant (K_F).

Since available models neglect device bulk resistance, a value for this parameter should be included in the circuit under study. The following discussion will provide a guideline to the impact of this parameter on circuit threshold analyses.

The bulk resistance is the resistance of the semiconducting material between the ohmic contacts and the junction of the semiconductor. In the normal operating regions of a diode or transistor, the voltage drop across the bulk resistance is small because of the low level currents involved and is normally not considered for small signal, low frequency problems. For currents on the order of those required to fail a semiconductor junction, the power dissipated in the bulk resistance may be a significant part of the total power.

The bulk resistance of a forward biased device is small (Reference 6) usually on the order of 0.1 to 10 ohms. The higher bulk resistances are associated with small area, low power devices which have limited current handling capabilities while the lower bulk resistances are associated with the higher power devices. The bulk resistance of a semiconductor device has been found to be larger in the reverse direction than in the forward direction (Reference 6). For reverse biased devices, the bulk resistance

may vary from 100 ohms to 10,000 ohms. In this case, the lower bulk resistances are generally associated with low breakdown voltages and the higher bulk resistances are generally associated with large breakdown voltages. This can be seen in Figure III-9 which shows a plot of bulk resistance for the reverse biased case versus device breakdown voltage for a limited sample of silicon diodes. The data presented were taken from a general listing given in Reference 4 and have been limited to the reverse bias case and levels below failure. In this figure one can see the trend to larger bulk resistance as the device breakdown voltage increases. Figure III-10 shows a plot of the bulk resistance for the reverse bias case versus device current for the same group of devices. The data, in general, show a decrease in bulk resistance with increasing current. The series of data points on the lower part of the graph are the low breakdown voltage devices.

For a forward biased junction near failure, the current will be large. The power dissipated in the junction will be small compared to power dissipated in the bulk resistance ($V_j << I_j R_B$). The device power can be approximated by:

$$P_D = I_j^2 R_{B_{FORWARD}}$$

Since for the forward bias case, the bulk resistance is much smaller than the source resistance, the source will look like a constant current. The power will then be directly proportional to the bulk resistance. To calculate the failure current, assuming the failure power is known ($P_F = Kt^{-1}$), a value for R_B must be determined. Little information is available on the bulk resistance of devices. One therefore has the option of measuring the device of interest or of estimating the bulk resistance. Since the power is directly proportional to bulk resistance, any estimate made should be large so that a conservative estimate of the current is obtained. Examples of such an estimate are 10 uhms for low power devices and 1 or 2 ohms for higher power devices.

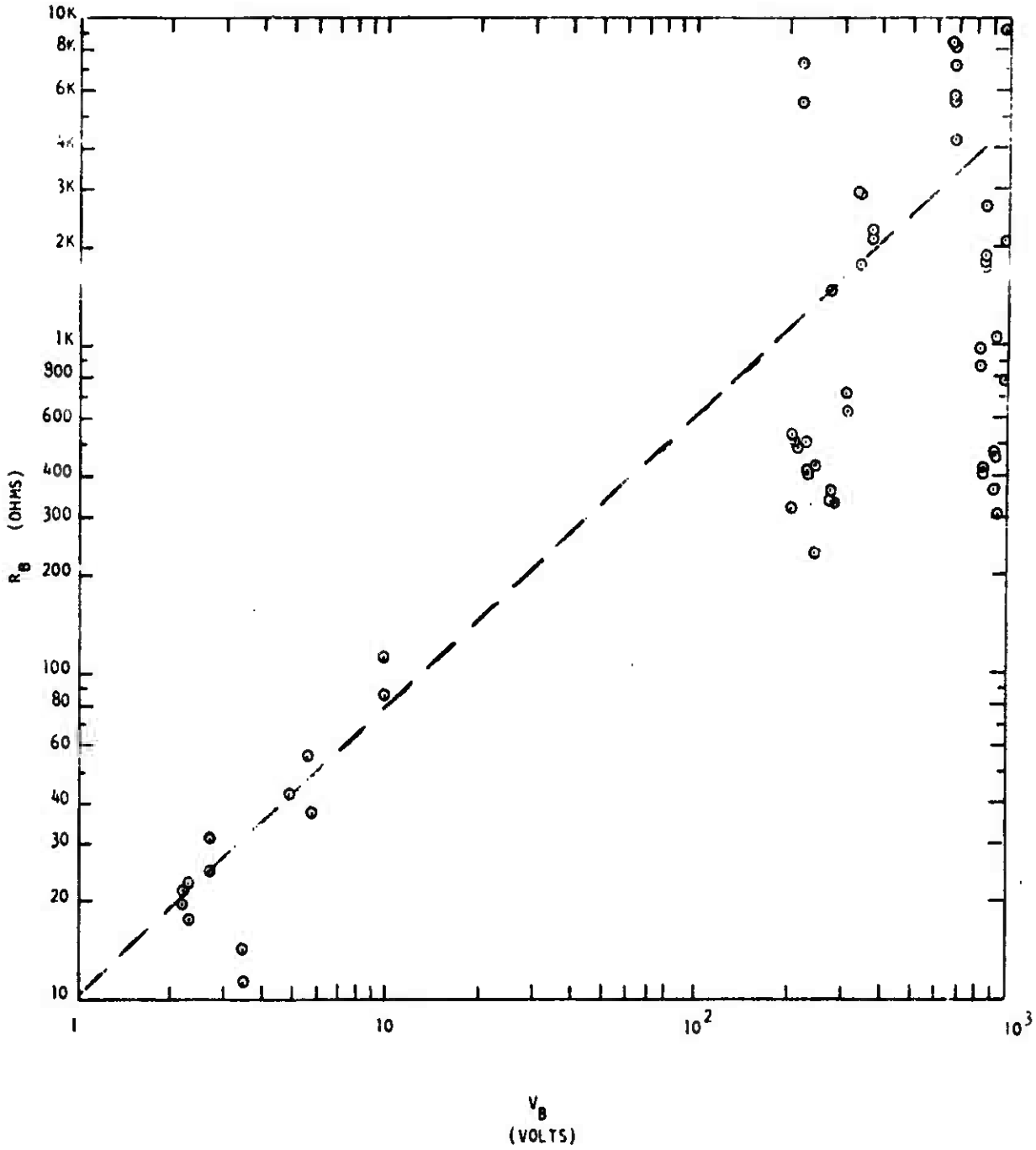


Figure III-9. Plot of Bulk Resistance for Reverse Biased Case Versus Device Breakdown Voltage

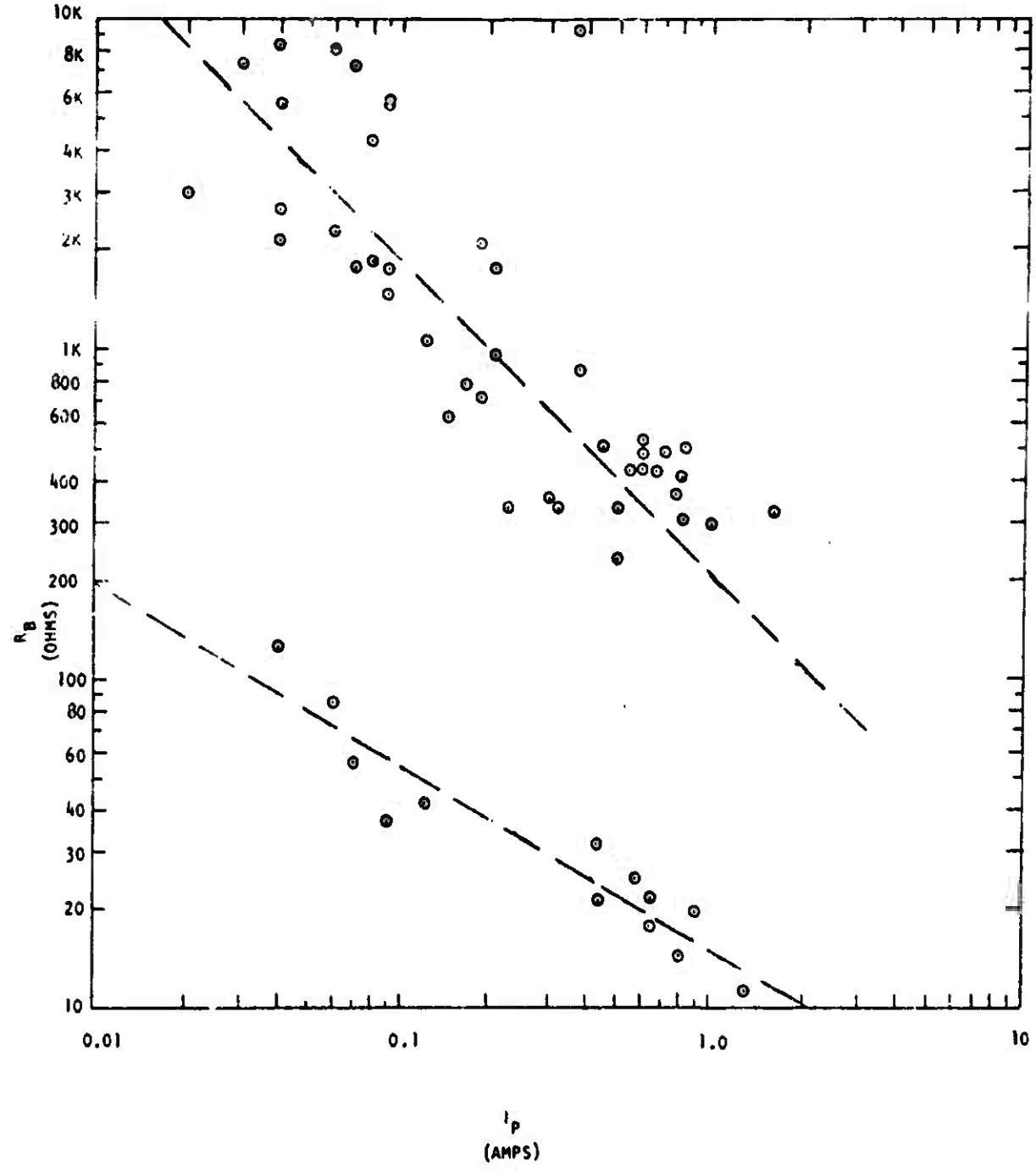


Figure III-10. Plot of Bulk Resistance for the Reverse Biased Case Versus Device Current

For reverse biased junction, the voltage drop across the bulk resistance may be neglected for low breakdown voltage, low current devices. In the case of higher breakdown voltage devices (larger bulk resistance), ignoring the bulk resistance will lead to conaervative estimates of circuit failure damage thresholds. For silicon diodes, bulk resistance estimates could be made by reference to Figure III-9.

In general, for low power, low breakdown voltage devices pulsed in the reverse direction, the bulk resistance can be ignored when making failure threshold estimates. For high breakdown voltage devices pulsed in the reverae direction and junctions pulsed in the forward direction, it is best to estimate a value of bulk resistance in order to obtain a realistic estimate of failure threshold. The sample problems presented later illustrate the effect of bulk resistance value on minimum signal amplitude required to produce damage.

As stated earlier, little is known about the transient damage characteristics of nonsemiconductor devices or newer types of semiconductor devices such as integrated circuits and field effect devices. With the increased use of low power, precision components, damage threshold analyses yielding excessive power dissipation in passive components should be examined carefully to isolate critical nonsemiconductor components.

Figure III-11 gives a comparison of device damage constants for various component types. To provide a basis for comparison, the Wunsch model was assumed to apply to all device types.

While component level transient response and failure mode data are most critical to a damage threshold analysis, other general information such as circuit component values and general transistor specifications is also required.

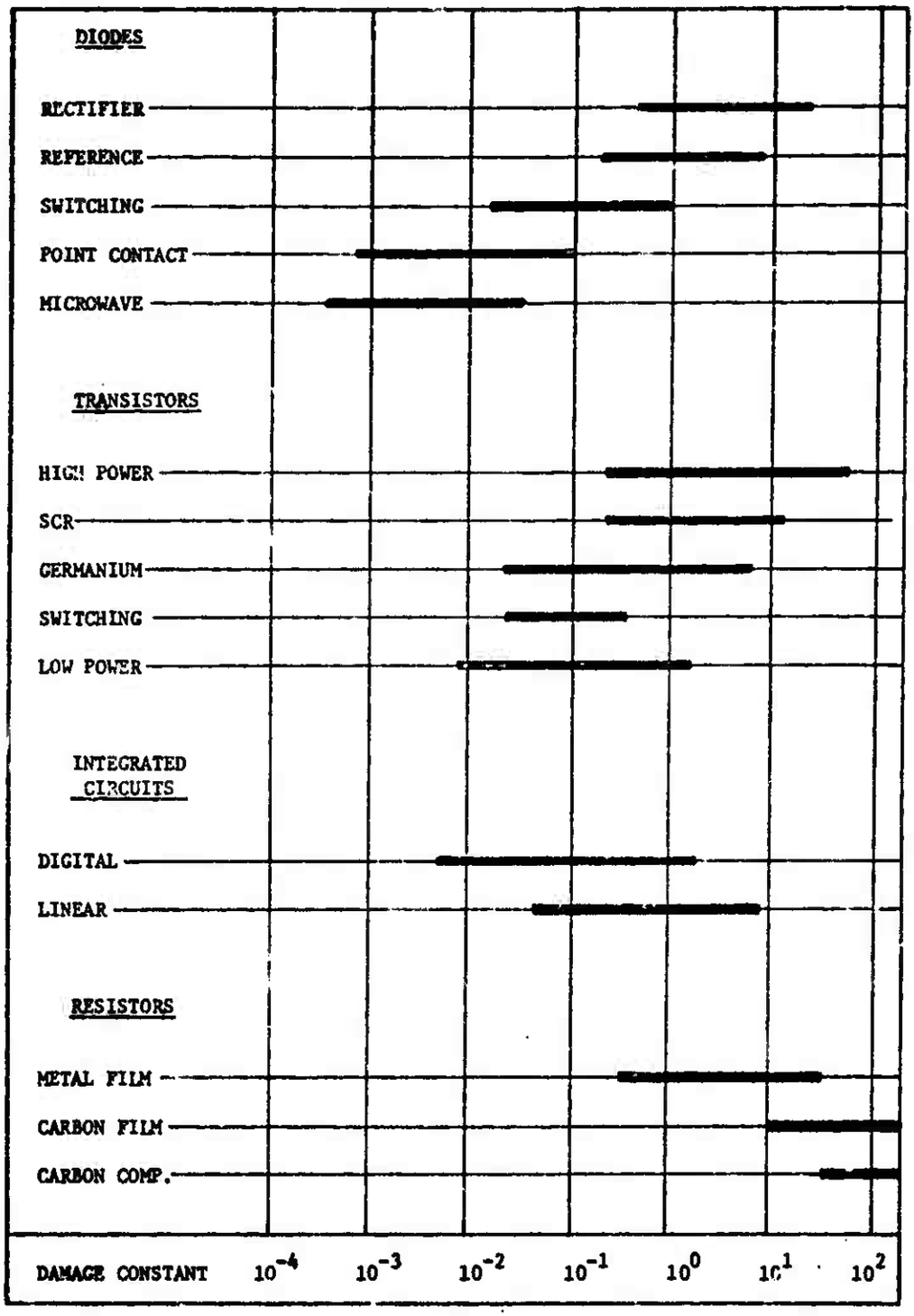


Figure III-11. Damage Constant Comparison of Varioua Component Types

As in the case of upset threshold analysis, device models required for damage analyses are very important and are discussed in detail in Appendix A.

5. DAMAGE ANALYSIS EXAMPLES

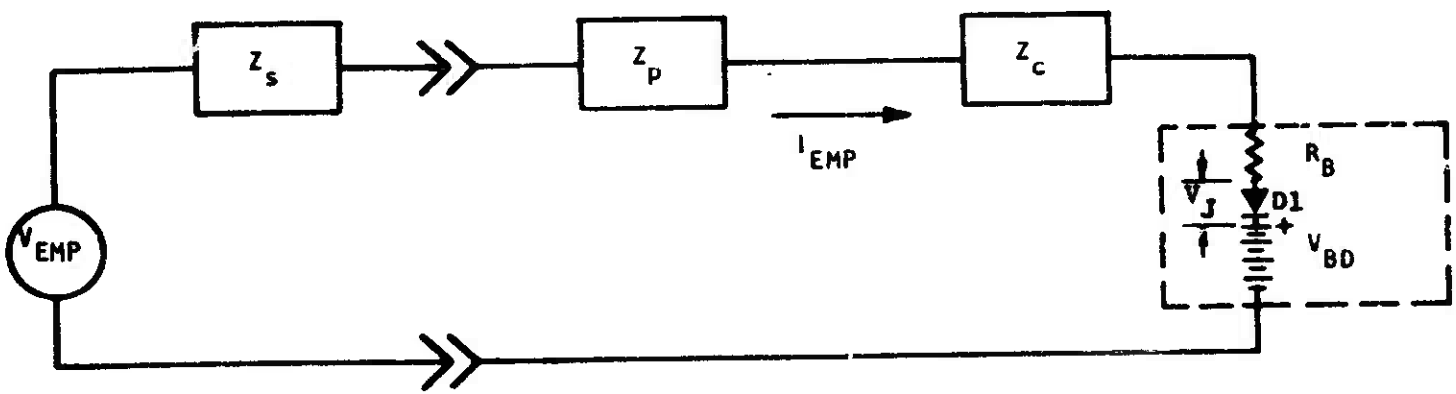
a. Hand Analysis

The detailed approach taken to determine the damage threshold of a given circuit node depends largely on the circuit complexity and available component data. The first step in any damage hand analysis is to simplify the circuit to a single loop, if possible, by inspection, using DPI techniques, breakpoint analysis, or Kirchoff's laws. DPI and breakpoint analyses are discussed in Appendices C and A, respectively. The other methods are assumed to be known by the reader. The examples presented later in this section illustrate several of the circuit simplification techniques mentioned above.

As stated earlier in this handbook, the EMP induced excitation for a given circuit may or may not be defined. Even if a specified driving function is not defined, a range of probable excitations can be defined such that a limited number of damage threshold solutions can be made and a curve relating voltage or power damage level to pulse widths or frequency can be plotted.

To illustrate the special problems associated with damage threshold analysis, the circuit shown in Figure III-12 will be used as a generic example. The circuit loop shown was defined by circuit simplification procedures and a junction is represented by its reverse breakdown equivalent circuit. Given a specific source configuration and signal, the current in the circuit is

$$I_{EMP} = \frac{V_{EMP} - V_{BD}}{Z_s + Z_P + Z_c + R_B}$$



V_{EMP} = EMP Signal
Z_s = Source Impedance
Z_p = Impedance of Circuit and Device Parasitics, i.e., Surge Impedance
Z_c = Impedance of Lumped Circuit Elements
R_B = Device Bulk Resistance
V_{BD} = Junction Breakdown Voltage

Figure III-12. Generic Circuit as an Example of Damage Analysis

If this current exceeds the magnitude required for device failure, for example, if

$$I_{EMP} > \frac{K_R t^{-1/2}}{V_{BD}} ,$$

then the probability is high that the junction will be damaged.

The above treatment assumes that Z_P is known, which is usually not the case, and that no lumped circuit elements (Z_c) will fail before the critical junction. If Z_c were a series resistor (R), and if the actual pulse power dissipated in the resistor was several orders of magnitude greater than its dc power rating, then potential damage to this element must be considered (as shown by Figure III-11).

Since little data are available describing bulk resistance, R_B must be estimated or neglected for most damage problems. As shown earlier, the bulk resistance of a reverse biased junction is a function of both breakdown voltage and junction current. In lieu of a measured or estimated value of R_B, worst case damage threshold (lowest signal amplitude) will be obtained by assuming zero bulk resistance for the reverse bias case and R_B equal to Z_s, maximum power transfer, for the forward bias case.

For a given EMP induced signal waveform and amplitude, the value of Z_s used for a given problem can determine failure mode and, therefore, must be carefully calculated or postulated for each problem. Example Problem 4 illustrates the importance of source impedance in solving damage problems.

If the waveform and amplitude of the EMP induced signal are not known exactly, a general graphical relationship between the damage power threshold and the incident pulse width (τ) or frequency (f) may be formulated by repeated circuit solutions. Figure III-13 shows both circuit and

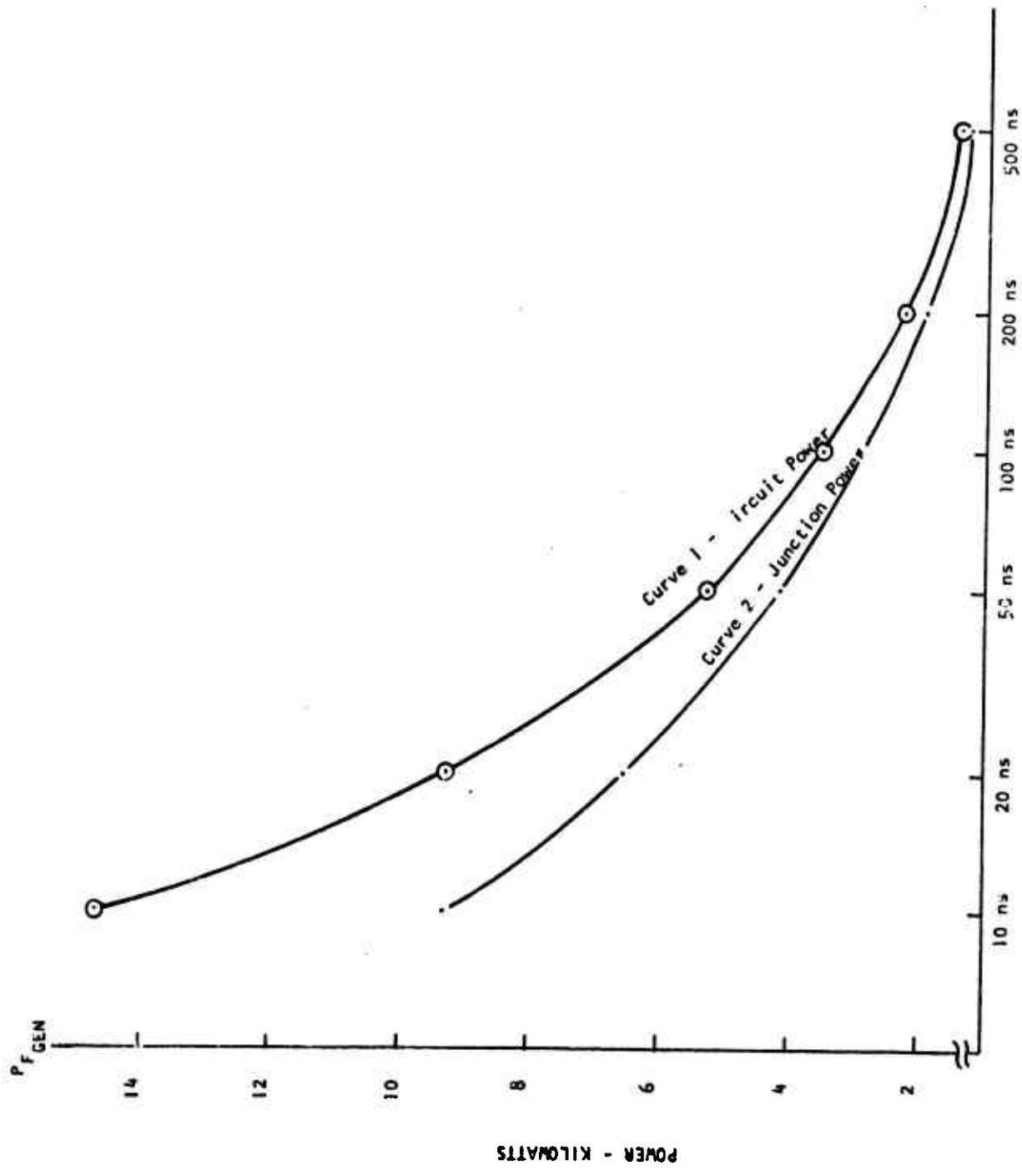


Figure III-13. Circuit and Junction Damage Level Power as Function of Pulse Width

junction damage level power as a function of pulse width for the circuit of sample Problem 1. Care must be taken for pulse widths less than spproximately 50 nanoseconds since Wunsch (Reference 1) indicates that junction burnout power varies as a function of τ^{-1} rather than $\tau^{-1/2}$ for short pulse durations. The curves of Figure III-13 will give a conservative estimate, however.

Each subsystem or circuit analyzed for damage threshold is unique and the use of one or more circuit simplification technique depends largely on the circuit configuration encountered. Most damage problems worked by hand analysis are solved using a combination of breakpoint and DPI techniques. Once experience is gained using these methods, many circuits can be simplified by inspection and the problem reduced to a few simple computations. At the present time, the limited pulse power burnout data available for most component types represent the main limitation of damage threshold analysis techniques. The following example problems are typical of the circuits that can be solved with the available component data base.

(1) Problem 1. Remote Controlled Relay

The first circuit chosen for analysis is a simple remote controlled relay. The relay coil has a diode across its terminals that may be EMP susceptible. This circuit is shown in Figure III-14. Assuming that the inductance of the relay coil is large, its impedance will be large compared to the diode impedance at frequencies in the one megahertz range. Therefore, the coil impedance will be neglected.

The failure current can be determined by:

$$I_F = \frac{P_F}{V_{BD}} = \frac{K_R t^{-1/2}}{V_{BD}}$$

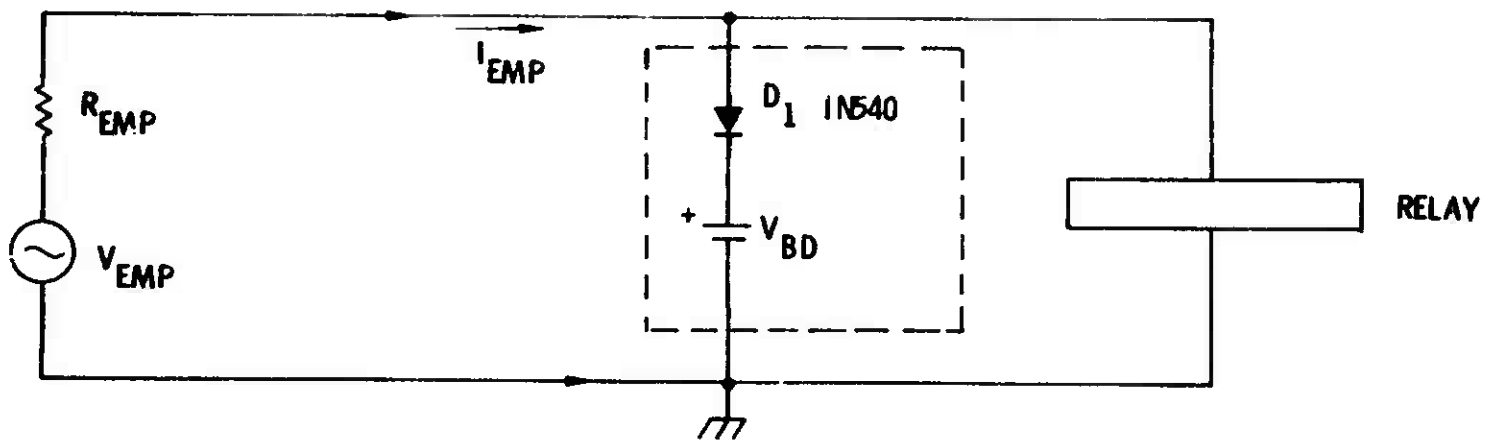


Figure III-14. Simple Remote Controlled Relay

For a IN540 diode, the reverse breakdown voltage, V_{BD}, is 400 volts and the damage constant, K, is 0.93 (see Appendix D). Using a 200 nsec pulse to approximate a 1 MHz damped sine wave (see Appendix B), the failure current for the diode is

$$I_F = \frac{0.93(2\times10^{-7})^{-1/2}}{400} = 5.2 \text{ amperes}$$

For a resistive source impedance of 10 ohms, the voltage required to produce this current is determined from Figure III-14 to be

$$V_{EMP} = V_{BD} + I_{EMP} R_{EMP} = 452 \text{ volts}$$

Therefore, a 452-volt, 200-nsec pulse, or a 1 MHz damped sine wave having a peak amplitude of 452 volts will cause the diode to fail.

The bulk resistance (R_B) of the IN540 diode was neglected in the above computation. If a bulk resistance of 10 ohms is assumed, then V_{EMP} for failure would be

$$V_{EMP_1} = V_{BD} + I_{EMP} (R_{EMP} + R_B) = 504 \text{ volts}$$

and one can see that neglecting bulk resistance gives a more conservative (lower) threshold prediction. The difference between V_{EMP} and V_{EMP_1} in this case is relatively small, but in general, the damage threshold voltage predicted with bulk resistance considered will be much higher than that predicted neglecting bulk resistance. This implies that hardening penalties may be minimized if accurate bulk resistance information were available such that realistic rather than ultraconservative threshold voltages could be determined.

(2) Problem 2. Phase Splitter Circuit

The circuit shown in Figure III-15 is a simple phase splitter amplifier utilizing one 2N706 transistor. The first step in determining the input required for damage is to simplify the circuit. For a frequency of 1 MHz, the impedances of C_1 and C_2 are 15.9 and 3.98 milliohms respectively. Since these impedsnces are small compared to the resistors in the circuits, C_1 and C_2 can be replaced by short circuits for the purpose of this analysis. Since dc powerlines are generally shunted by large filter capacitors, the 12-volt power supply line can be considered to be at ac ground potential. The resultant circuit after simplification is shown in Figure III-16.

The circuit can be further simplified by determining equivalent resistances for the base circuit and for the collector circuit. The base-emitter junction and the base-collector junction are also replaced by their diode equivalents to rspresent the breakdown region. This simplified circuit is shown in Figure III-17. Also shown in Figure III-17 are the breakdown voltages and damage constants for the 2N706. Note that for the 2N706, a damage constant for the collector-bsse junction is available.

The circuit is now simplified to the point where it lends itself easily to hand analysis. The next step is to determine which device will fail and what is the failure mods. The passive components are generally abls to withstand higher energies than transistors for short duration pulses, therefore, the transistor is the element to consider for damage. Failure is also assumed to occur in the reverss biased direction.

Using the Wunsch damage model ($P = Kt^{-1/2}$), a calculation is made to see whether the emitter-base junction or the collector-bsse junction will fail at the lower power. Using a pulse duration of 200 nsec,

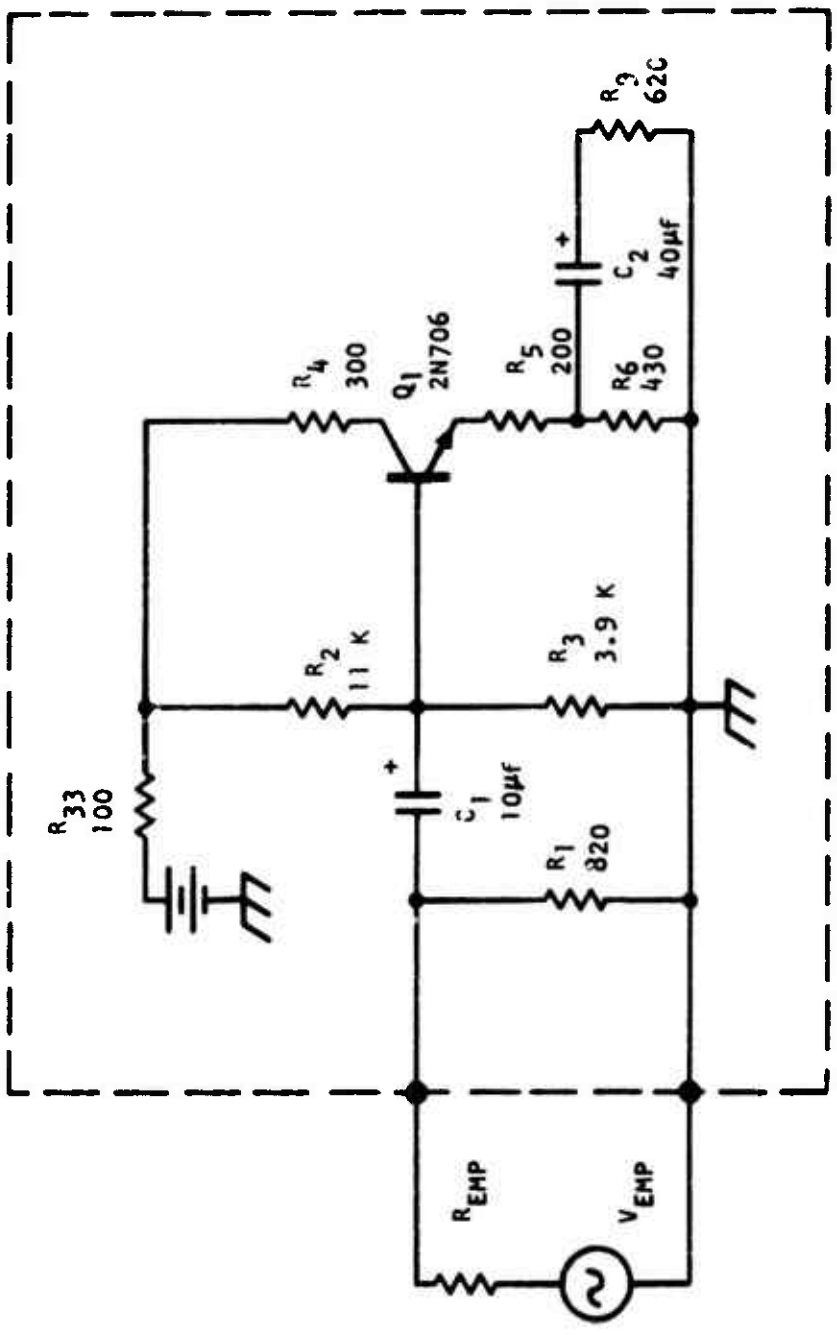


Figure III-15. Phase Splitter Circuit

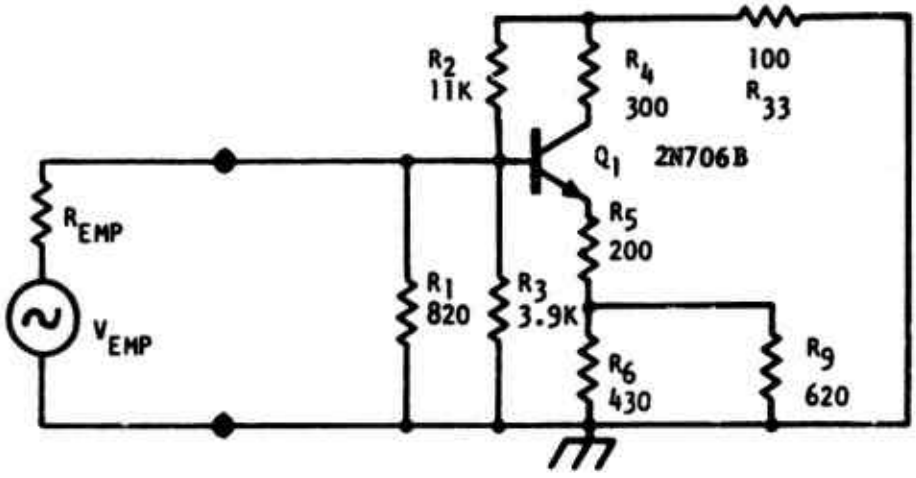
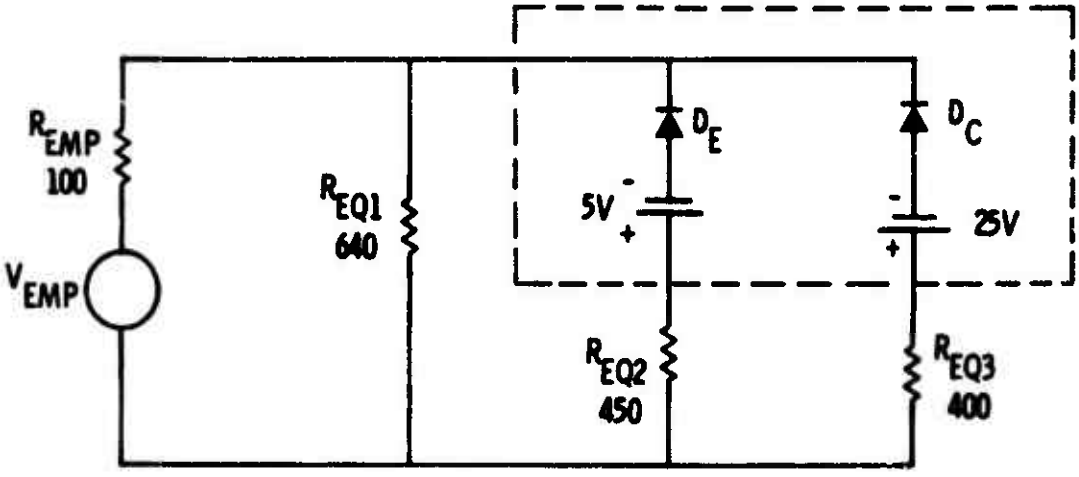


Figure III-16. Simplified Phase Splitter Circuit



2N706: K_{EB} = 0.0075 watt-sec$^{1/2}$ BV_{EBO} = 5V

K_{CB} = 0.058 watt-sec$^{1/2}$ BV_{CBO} = 25V

Figure III-17. Further Simplification of Phase Splitter Circuit

$$P_{EB} = K_{EB} t^{-1/2} = 16.77 \text{ watts}$$

$$P_{CB} = K_{CB} t^{-1/2} = 129.7 \text{ watts}$$

This calculation shows that the emitter-base junction is the most susceptible. The current required to fail the emitter-base junction (I_{EB}) is

$$I_{EB} = \frac{P_{EB}}{V_{BD}}$$

$$I_{EB} = 3.35 \text{ amperes}$$

The voltage from the base to ground is

$$V_{BASE} = BV_{EBO} + I_{EB} R_{EQ2}$$

$$V_{BASE} = 1.51 \text{ kV}$$

The current through the collector-base junction is

$$I_{CB} = \frac{V_{BASE} - BV_{CBO}}{R_{EQ3}}$$

$$I_{CB} = 3.71 \text{ amperes}$$

The power dissipated in the collector-base junction is

$$P_{CB} = BV_{CBO} \cdot I_{CB}$$

$$P_{CB} = 93 \text{ watts}$$

which is below its failure threshold power. The total current into the circuit is

$$I_{EMP} = I_{JF} + I_{CB} + \frac{V_{BASE}}{R_{EQ1}}$$

$$I_{EMP} = 9.41 \text{ amperes}$$

and the EMP generator voltage, assuming a 100 ohm resistive source impedance, is

$$V_{EMP} = V_{BASE} + I_{EMP} R_{EMP}$$

$$V_{EMP} = 2.45 \text{ kV}$$

Therefore, for a 100 ohm source impedanca, a 2.45 kV, 200 nsec pulse will cause the transistor to fail. Note that more thsn 2000 watts will be dissipated in R_5 and potential damage to this component should be considered.

Another method of computing V_{EMP} and I_{EMP} needed for failure is to write the loop equations for the loops shown in Figure III-18.

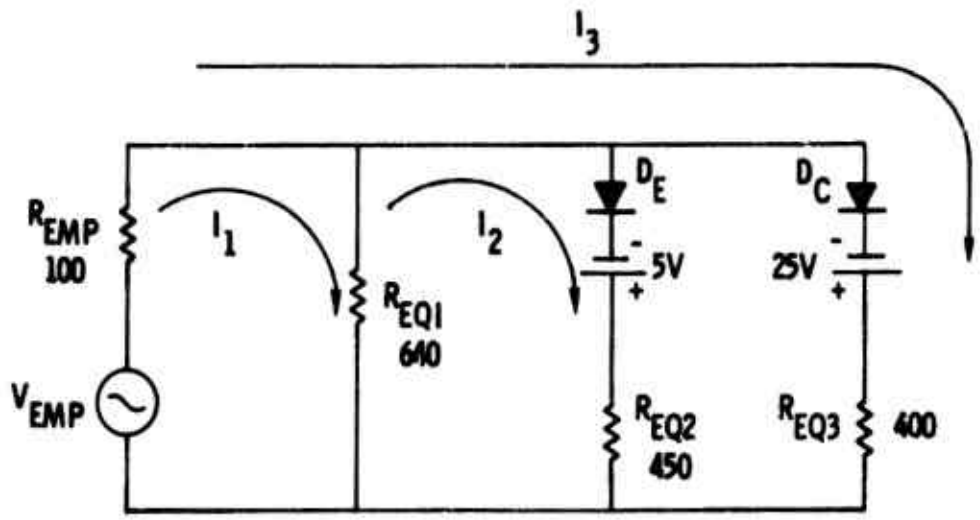


Figure III-18. Phase Splittar Circuit Showing Current Loops

$$\text{(loop 1)} \quad I_1(R_{EMP} + R_{EQ1}) - I_2(R_{EQ1}) + I_3(R_{EMP}0 = V_{EMP}$$

$$\text{(loop 2)} \quad -I_1(R_{EQ1}) + I_2(R_{EQ1} + R_{EQ2}) + I_3(0) = BV_{EBO}$$

$$\text{(loop 3)} \quad I_1(R_{EMP}) + I_2(0) + I_3(R_{EMP} + R_{EQ3} = V_{EMP} - BV_{CBO}$$

Solving for I_2, one obtains

$$I_2 = \frac{V_{EMP}}{733}$$

From the previous calculstion, 3.35 amps are required to fail the emitter-base junction. By inspection of Figure III-18, the emitter-base current is I_2. Therefore,

$$I_2 = \frac{V_{EMP}}{733} = 3.35 \text{ amperes}$$

and

$$V_{EMP} = 2.46 \text{ kV}$$

This answer, computed by solving the simultaneous loop equations, sgrees with the first method which was a "brute force" current divider spproach.

(3) Problem 3. Push-Pull Amplifier

The circuit shown in Figure III-19 is a push-pull amplifier where the output has been found to be the point exposed to EMP induced transieuts. Before proceeding with the calculation of the failure currents and voltsges, the circuit will be simplified.

The two overload protection lamps shown in Figure III-19 will have s transient response time much slower than the 200 nsec pulse width sssumed for this problem. The overlosd protection lamps can be

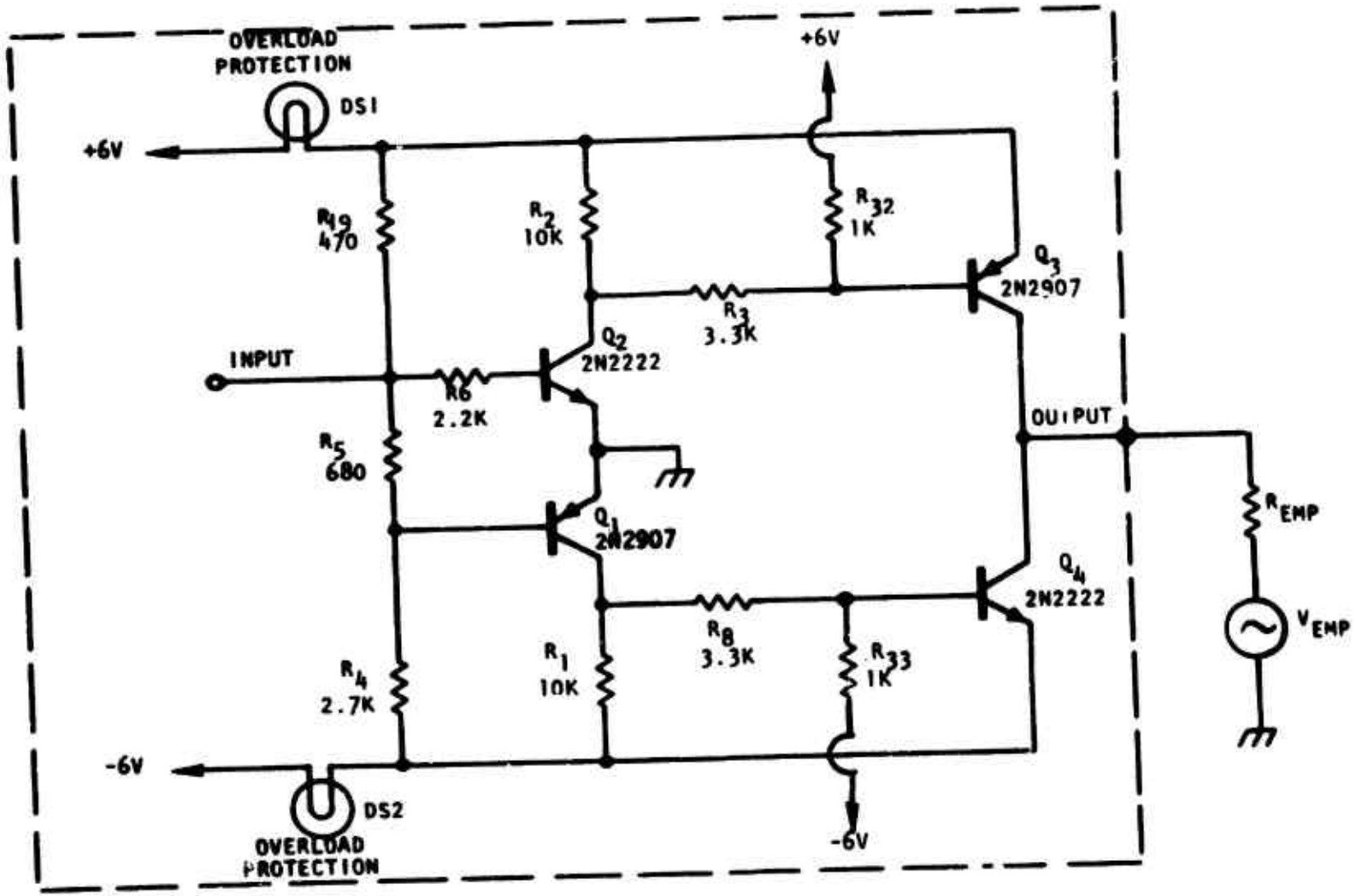


Figure III-19. Push-Pull Amplifier Circuit

replaced by resistors whose value is approximately the "cold" resistance of the lamps. For this analysis, this value will be assumed to be 10 ohms. The power supply lines can also be assumed to be at ac ground potential. The circuit with the above simplifications is shown in Figure III-20.

Since the EMP generator is connected to Q_3 and Q_4, one of these devices is most likely to fail. Note that R_3 and R_8 serve to limit the current through Q_1 and Q_2 due to a transient appearing at the base of Q_3 or Q_4. This may be further simplified by obtaining an equivalent resistance for the base-emitter circuit of Q_3 and Q_4. The driving point impedance looking from the base of Q_3 or Q_4 back into the circuit is

$$DPI_B = 1\ K\ ||\ [3.3\ K + 10\ K\ ||\ (R_{cc} + 10)]$$

R_{cc} is the impedance of Q_1 or Q_2 from collector to ground and should be on the order of 50 K to 100 K ohms. The DPI will then be approximately equal to 1000 ohms and this is the equivalent base-emitter resistance of Q_3 or Q_4. The simplified circuit is shown in Figure III-21. Also shown in Figure III-21 are the pertinent device parameters needed for the failure calculstions.

A positive EMP transient will forward bias the collector-bsse junction of Q_3. The 1 K resistor in the base of Q_3 will limit this current. Once the emittar-base breakdown voltage of Q_3 has been exceeded, a current path from the collector to the emitter is astablished snd failure can occur in the emitter-base junction. The collector-base junction of Q_4 could also be in breakdown with its emitter-base junction forward biased; however, the failure thresholds for the forward biased emitter-base junction and the revarse-biased collector-base junction are both largar than the reverse biased emitter-base junction. Therefore, for a positive transient, the emitter-baaa junction of Q_3 will probably fail. For a nagativa tranaient, failure can ba determined by interchanging Q_3 and Q_4 in tha preceding discuasion. This circuit is an example of failure occurring at the same level for an input transient of either polarity.

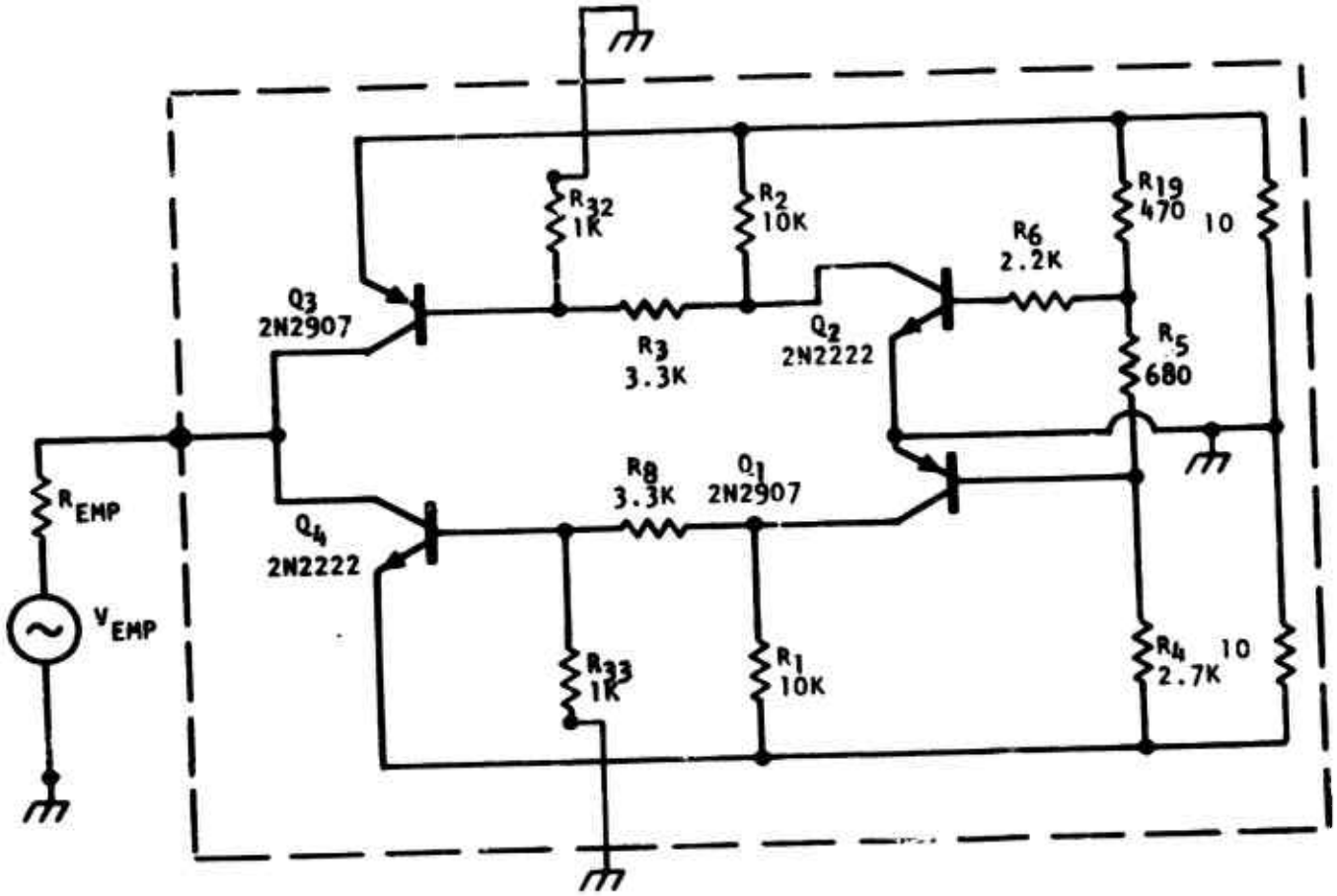
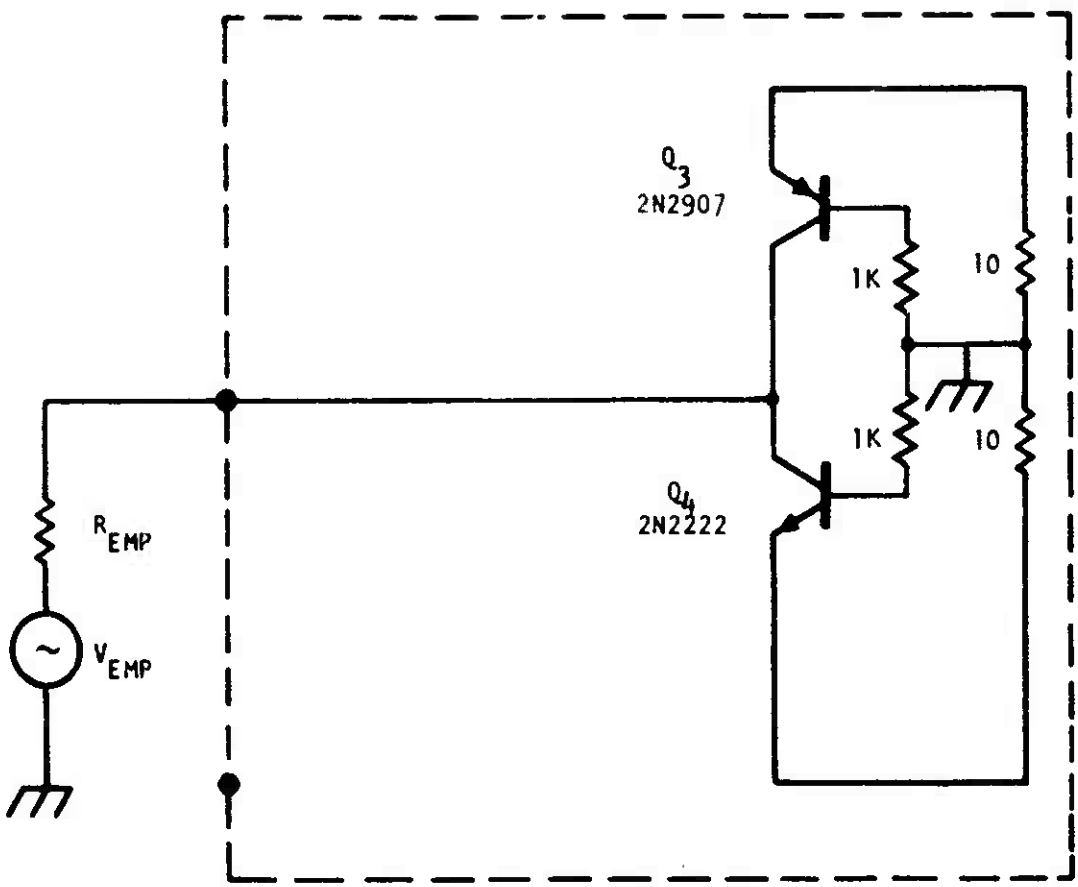


Figure III-20. Simplified Push-Pull Amplifier Circuit



2N2222 and 2N2907: K_{EB} = 0.1 watt-sec$^{1/2}$

BV_{EBO} = 5 volts

BV_{CBO} = 60 volts

Figure III-21. Push-Pull Amplifier Circuit With Additional Simplifications

The current required to fail the emitter-base junction of Q_3 for a 200 nsec pulse is

$$I_F = \frac{K_{EB}(2\times10^{-7})^{-1/2}}{BV_{EBO}}$$

$$I_F = 45 \text{ amperes}$$

The voltage from the collector of Q_3 to ground is

$$V_{C_3} = BV_{EBO} + 10(I_F)$$

$$V_{C_3} = 455 \text{ volts}$$

The current flowing through Q_4 and the 10 ohm resistor from its emitter to ground is

$$I_{Q_4} = \frac{V_{C_3} - BV_{CBO}}{10}$$

$$I_{Q_4} = 39.5 \text{ amperes}$$

The current through the 1000 ohm resistors has been neglected. The total input current is

$$I_{EMP} = I_{Q_4} + I_F$$

$$I_{EMP} = 84.5 \text{ amperes}$$

and, assuming a 10 ohm resistive source impedance, the EMP generator voltage is

$$V_{EMP} = V_{C_3} + I_{EMP}R_{EMP}$$

$$V_{EMP} = 1300 \text{ volts.}$$

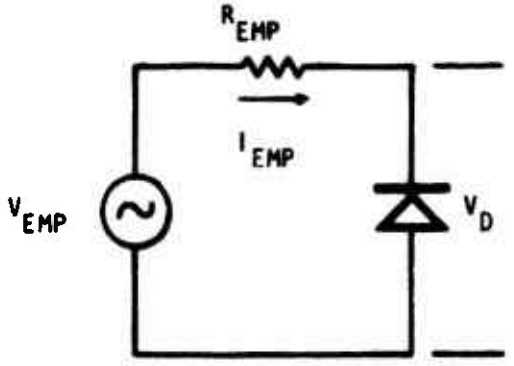
Although the semiconductor devices exposed to transient damage were found to be quite insensitive, it should be noted thst considerable power is dissipsted in the overload protection lamps and that potential damage to these or other nonsemiconductor components should be considered before making a relative susceptibility statement.

(4) Problem 4. Specisl Example to Illustrate Source Impedance Effects

This damage snalysis example has been chosen to illustrste the effect of the source impedance on the failure mode of a simple diode circuit. The diode parameters hsve been specislly chosen; however, they are reslistic vslues. The circuit to be used snd the diode psrameters are shown in Figure III-22. The bulk resistance is given for the forward direction since, for large currents, most of the power will be dissipated in the bulk. By comparing the damsge constants for the forward and reverse directions, one csn see that the device is hsrder in the forwsrd direction, as predicted by Wunsch and others.

The forwsrd and reversa damage constants, forward bulk resistanca and breakdown voltage were chosen based on s review of limited exparimantal dsts. Bulk resistance in the reverse biss direction is neglected as in previous cases.

For the first calculation, assume a source impedance, R_{EMP}, of 10 ohms. The failure current for reversa failure using s 200 nsec pulse is



DIODE PARAMETERS: K_R = 0.033 watt-sec$^{\frac{1}{2}}$
V_{BD} = 150 volts
K_F = 0.089 watt-sec$^{\frac{1}{2}}$
$R_{B_{FWD}}$ = 2 ohms

Figure III-22. Circuit to Illustrate Source Impedance Effects

$$I_{F_{REV}} = \frac{K_R t^{-1/2}}{V_{BD}}$$

$$I_{F_{REV}} = 0.49 \text{ amp}$$

The EMP generator voltage is

$$V_{EMP} = V_{BD} + I_{F_{REV}} \cdot R_{EMP}$$

$$V_{EMP} = 155 \text{ volts.}$$

This is not, however, the lowest failure voltage. Consider now, the case of failure in the forward direction. Since in the forward bias case most of the power is dissipated in the bulk resistance, then

$$P_{FWD} \approx (I_{FWD})^2 R_B \approx K_F t^{-1/2}$$

therefore,

$$I_{F_{FWD}} = \sqrt{\frac{K_F t^{-1/2}}{R_B}}$$

$$I_{F_{FWD}} = 10 \text{ amperes}$$

and the EMP generator voltage is

$$V_{EMP} = I_{F_{FWD}} (R_B + R_{EMP})$$

$$V_{EMP} = 120 \text{ volts.}$$

The voltage required for failure is lower for the forward case. In fact, reverse failure would not occur since the voltage for forward failure is less than the reverse breakdown voltage.

For the next calculations, assume a source impedance, R_{EMP}, of 100 ohms. The failure current for reverse failure using a 200 nsec pulse is, from the previous calculation, 0.49 amperes and the EMP generator voltage is

$$V_{EMP} = V_{BD} + I_{F_{REV}} \cdot R_{EMP}$$

$$V_{EMP} = 199 \text{ volts.}$$

In this case, this is the lowest failure voltage. With the diode in the forward direction, the current through it for 199 volts EMP generator voltage is

$$I_{FWD} = \frac{V_{EMP}}{R_B + R_{EMP}}$$

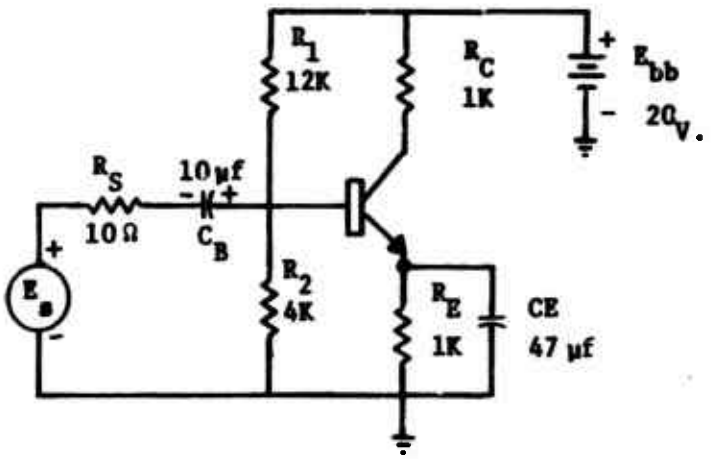
$$I_{FWD} = 1.95 \text{ amperes}$$

which is well below its failure threshold of 10 amperes.

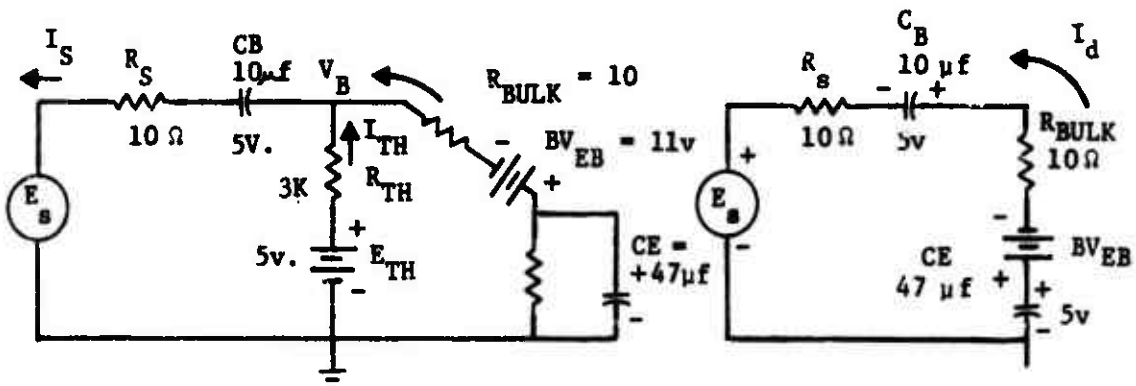
The preceding example illustrates that the source impedance can have an effect on the failure level and failure mode of a device. It also indicates that the device with the smallest damage constant will not always be the first to fail.

(5) Problem 5. Amplifier Circuit

The amplifier circuit shown in Figure III-23 was analyzed to illustrate a general circuit simplification procedure incorporating



(a) CIRCUIT DIAGRAM.



(b) Equivalent Circuit for Negative EMP

(c) Simplified Equivalent Circuit for Negative EMP

Figure III-23. Simplification of Amplifier Circuit

several techniques. A negative EMP signal is used in conjunction with a 10 ohm resistive source impedance. The equivalent circuit in Figure III-23(b) has been modified as follows:

(1) Neglect R_c since $R_c >> Z_E$

(2) Replace R_1 - R_2 voltage divider by its Thevenin equivalent circuit

(3) Replace the base emitter junction with its reverse breakdown equivalent circuit. A bulk resistance of 10 ohms is assumed.

A simplified equivalent circuit, shown in Figure III-23(c), will be used for comparison with the circuit shown in Figure III-23(b).

There are two energy-storage elements; however, since R_{TH} = 3K ohms is large compared to R_S = 10 ohms and R_{BULK} = 10 ohms, we can approximate the circuit as shown in Figure III-23(c) for purposes of computing the circuit's time constant. The time constant is

$$T = (R_S + R_{BULK}) \frac{C_B C_E}{C_B + C_E} = (20)\ (8.245\ \mu F) = 164.9\ \mu s$$

where the equivalent capacitance is represented by the series combination of C_B and C_E. If the EMP transient has a duration of 200 nsec, then the capacitor voltages will not change appreciably during the pulse. We are therefore justified in considering the capacitors as equivalent batteries whose voltage is equal to the capacitor's charge prior to the EMP arrival. We will subsequently demonstrate that the capacitor charges in this case can be neglected entirely.

$$P_d = (BV_{EB})\ (I_d) = K\ t^{-1/2}$$

where the following values are given for this test transistor

$$K = 0.1 \text{ wstt-sec}^{1/2}$$

BV_{EB} = base-emitter reverse breakdown voltage

= 11 volts

I_d = current required to damage the transistor for a given pulse width, t.

t = 200 nsec.

we find

$$I_d = \frac{Kt^{-1/2}}{BV_{EB}} = \frac{(0.1)\ (.2\text{x}10^{-6})^{-1/2}}{(11\ V)} = 20.3 \text{ amps}$$

Using Kirchoff's current and voltage laws, one may work backwards from the base-emitter junction to find the value of E_S which will cause the magnitude of I_d given above. Referring to Figure III-23(b) and considering the emitter voltage to be constant at V_{EQ}, we find the base voltage as the sum of the voltage drops through the base-emitter loop.

$$V_B = + V_{EQ} - BV_{EB} - I_d R_{BULK}$$

$$V_B = + 5\ V - 11\ V - (20.3)\ (10\Omega)$$

$$V_B = -209.3 \text{ volts}$$

At the base node a small current is required by the base biasing equivalent circuit. This current I_{TH} is found as

$$I_{TH} = \frac{V_{TH} - V_B}{R_{TH}} = \frac{5 + 209.2789}{3K}$$

$$I_{TH} = .0714 \text{ amps}$$

It is obvious that I_{TH} can be neglected in compariaon to I_d.

At the base node, it follows from Kirchoff's current law that

$$I_S = I_d + I_{TH} = 20.4 \text{ amps}$$

The value of E_S is therefore

$$E_S = -I_s R_s - V_{CB} + V_B = -418.3 \text{ volts}$$

Thus, if the EMP signal $E_S = -418.3$ volts and the pulse duration is 200 nsec, the transistor will be damaged.

Returning to Figure III-23(c) which shows the approximate equivalent circuit neglecting the base biasing network, we see that

$$E_S \simeq V_{EQ} - BV_{EB} - I_d R_{BULK} - V_{CB} - I_d R_S$$

$$E_S \simeq - 417.6 \text{ volts}$$

which differs from the value given earlier by only 0.17 percent. Thus, we see why it is often permissible to neglect the effect of base-biasing resistors in comparison to the source and bulk resistance terms. Also, we should note that V_{EQ} and V_{CB}, the capacitor charges, essentially offset one another. Therefore, one might often neglect initial capacitor charges, especially if their voltages counteract one another of if their initial charge is small compared to the EMP transient amplitude.

If the bulk resistance were neglected, then

$$E_{S_1} = V_{EQ} - BV_{EB} - V_{CB} - I_d R_S$$

$$E_{S_1} = -214 \text{ volts}$$

Voltage E_{S_1} is seen to be much more conservative (lower) than E_S. Neglecting bulk resistance would therefore overstate the hardening required for this circuit.

b. Computer-Aided Analysis

The phase splitter circuit studied in the previous section using hand analysis techniques and presented as Problem 2 was used to illustrate the applicability of circuit analysis computer codes to the damage threshold prediction problem. As in the upset case, CIRCUS 2, NET-2, and SCEPTRE (References 9 - 11) were used for purposes of demonstration.

The problems relating to device models and device libraries as discussed relating to the computer analysis of transient upset problems also apply to damage threshold problems. The device model problem is more severe for the damage case where semiconductor elements are being driven into areas where they would normally never operate. Device models must therefore represent the devices in both its normal region of operation and under conditions of high current injection and reverse breakdown. Models for bipolar transistors and diodes operating under these conditions are discussed in Appendix A and in more detail in References 12 and 15. For the phase splitter problem, the Ebers-Moll or change control models in the three codes were modified to include breakdown models across each device junction. This approach permits the use of existing device libraries whereas the use of a high current injection model requires some additional parameters.

Circuit schematics with nodes identified for formatting are shown in Figures III-24 and III-25. As in the hand analysis case, the objective of the computer-aided analysis was to determine the power dissipated in sensitive components and to compare diasipated power with power required for component burnout. Since damage threshold problems are generally performed with the circuit in a static (power off) mode, no initial condition problems are encountered.

For the example analyses a 200 nanoaecond variable amplitude pulse was applied through C_1 to the base of Q_1. Pulse rise and fall times of 10 nanoseconds were used. The power dissipated in the base-emitter and collector-base junctions was determined as a function of input amplitude and plots of these relationships were made. Figures III-26 and III-27 show junction power as a function of pulse amplitude for the three codes used. To determine the circuit damage threshold, the actual junction power must be compared with the junction failure power as predicted by the Wunsch model. From the calculations performed in the hand analysis aection, it is known that

$$P_{e-b} = 16.77 \text{ Watts}$$

$$P_{c-b} = 129.7 \text{ Watts}$$

Locating these points on the curves of Figures III-26 and III-27 yielded the data presented in Table III-1. This table shows that the e-b junction power will exceed its damage threshold st a lower circuit input signal (V_{EMP}) level than the c-b junction. Therefore, one may conclude that there is a high probability that the e-b junction failure will result in permanent circuit damage.

The method currently used in the computer-aided determination of circuit input voltage required to produce damage consists of three steps:

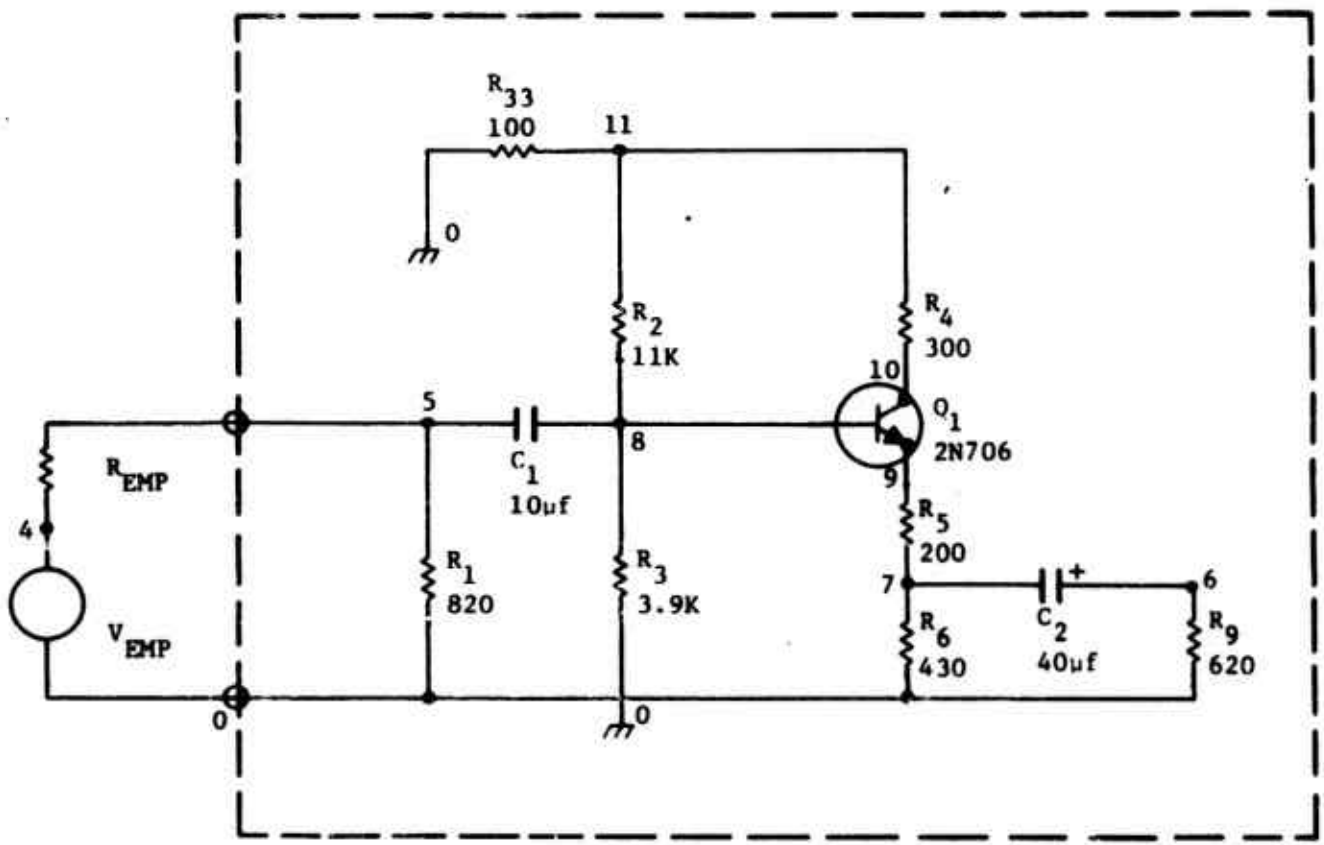


Figure III-24. Phase Splitter Circuit with Nodes Marked as Used for SCEPTRE and NET-2

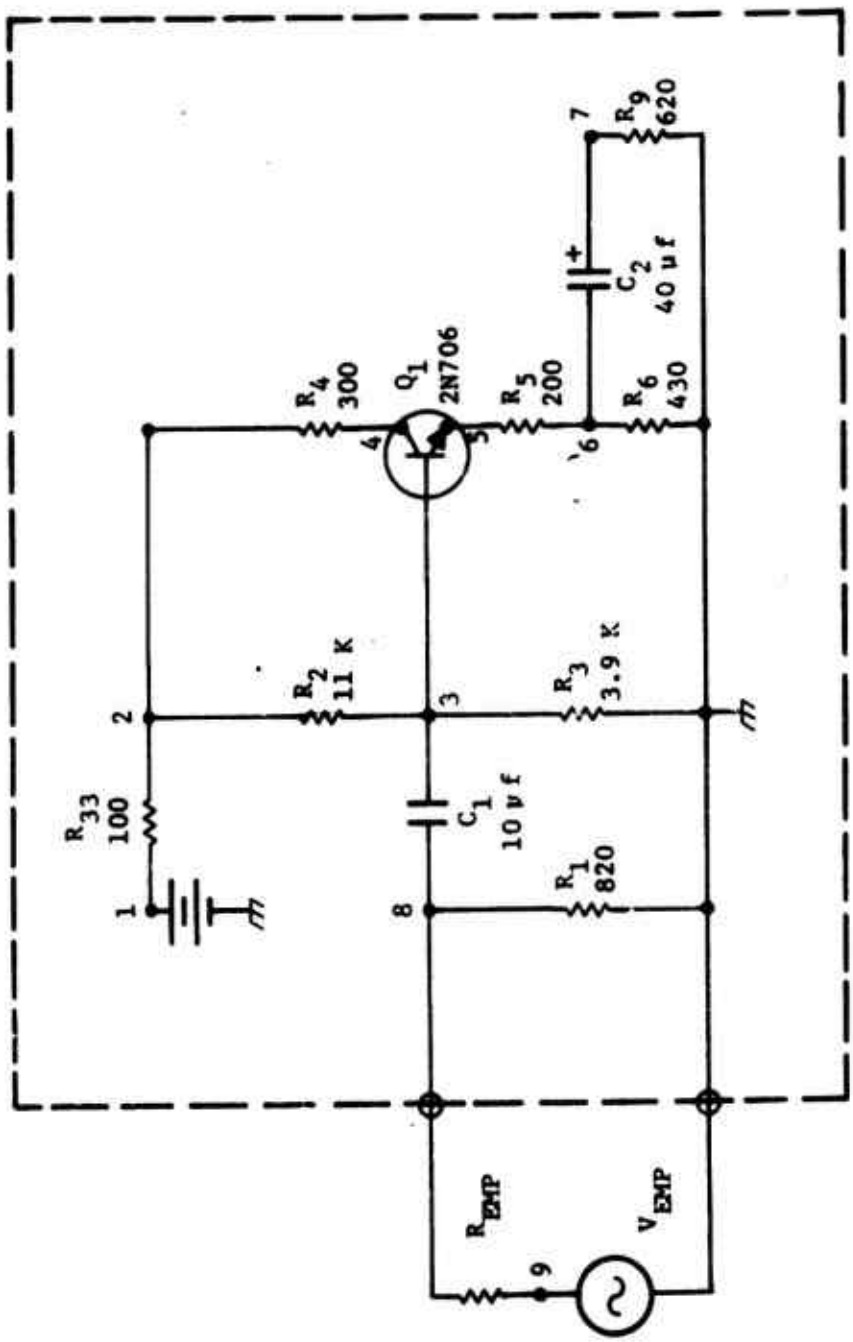


Figure III-25. Phase Splitter Circuit with Nodes Marked as Used for CIRCUS 2

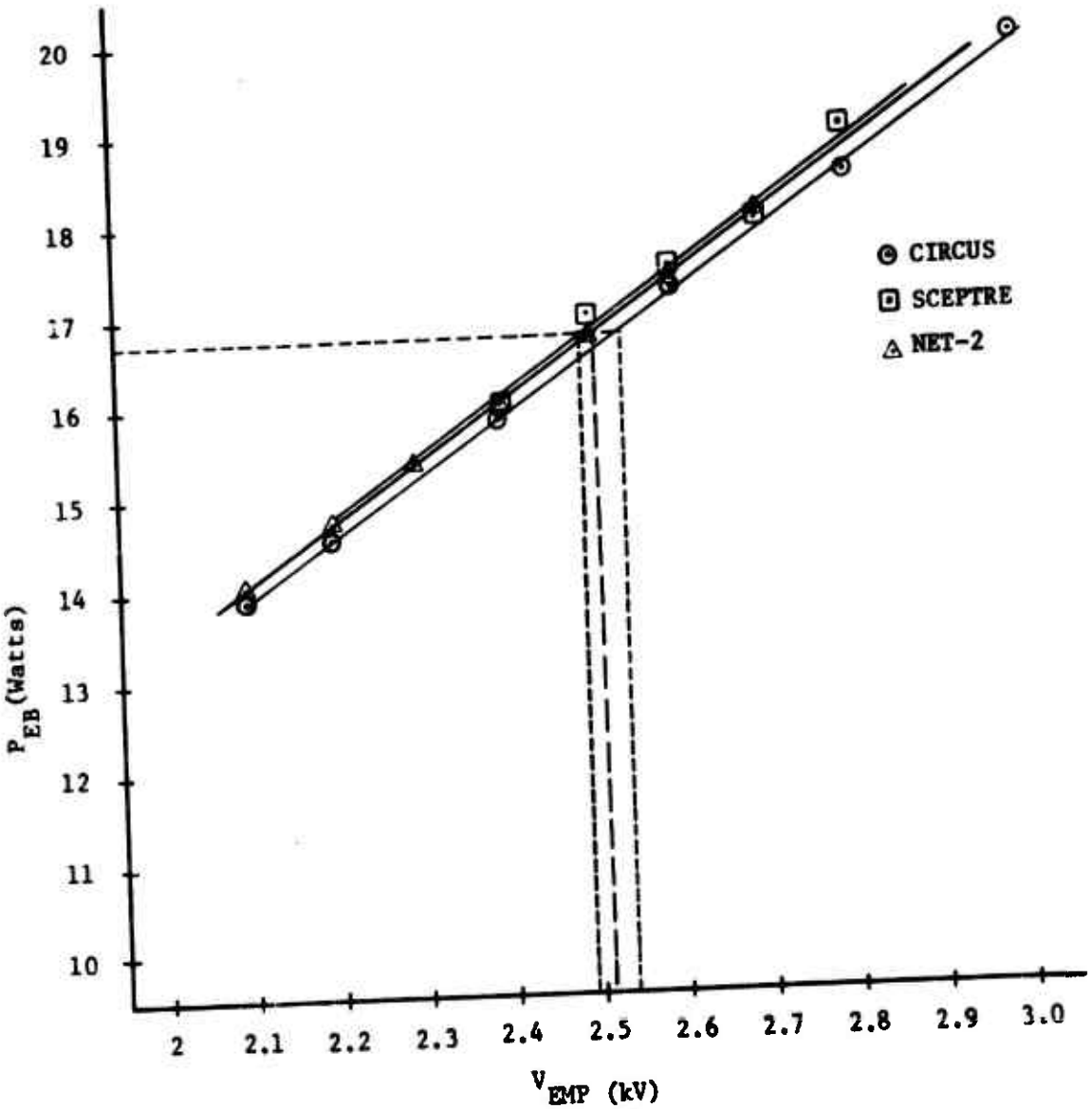


Figure III-26. Emitter-Base Power Versus Input Voltage

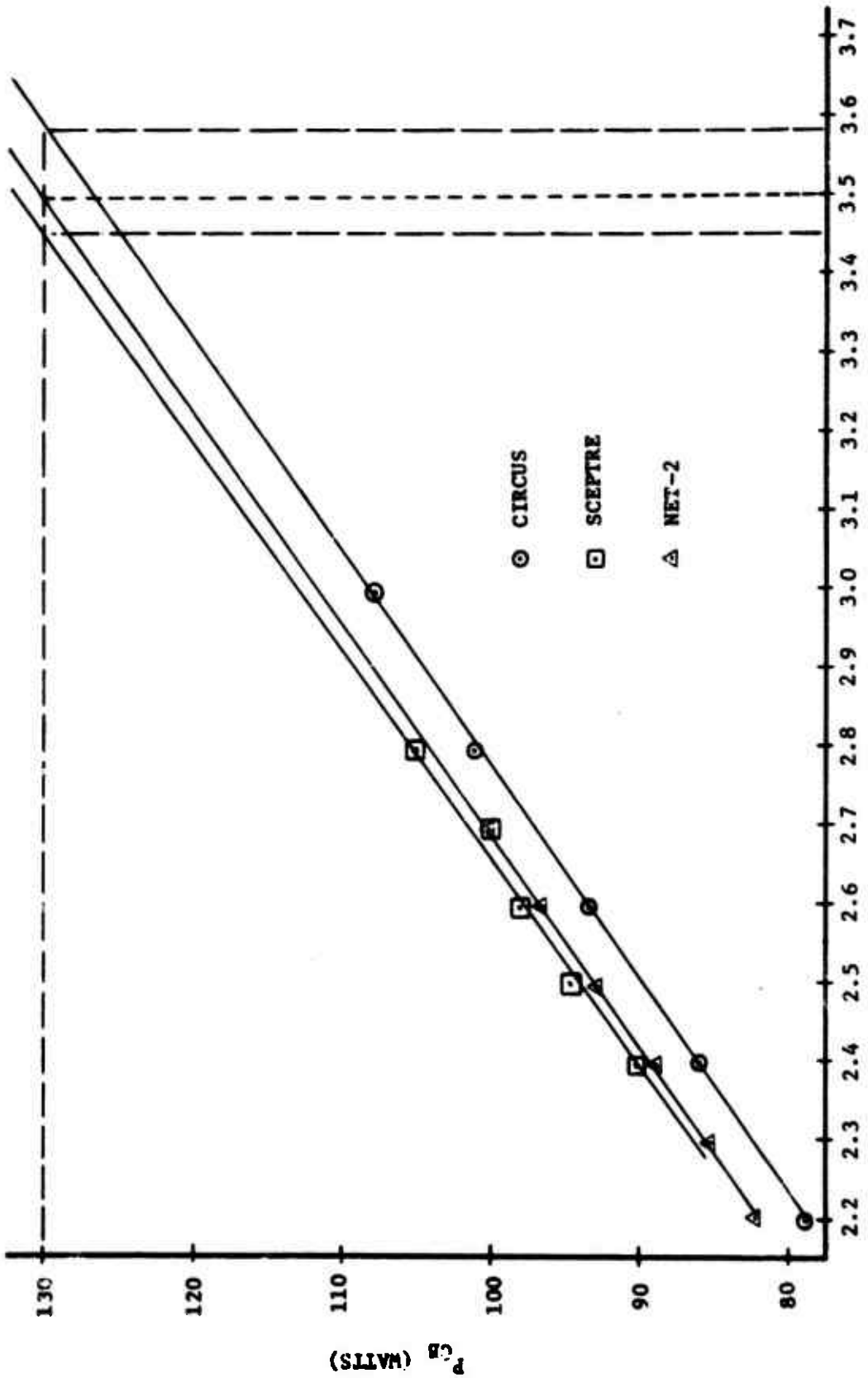


Figure III-27. Collector-Base Power Versus Input Voltage

TABLE III-1

SUMMARY OF DAMAGE THRESHOLD ANALYSIS RESULTS

	CIRCUS 2	NET 2	SCEPTRE	HAND ANALYSIS
V_{EMP} e-b Failure	2540 Volts	2510 Volts	2490 Volts	2450 Volts
V_{EMP} c-b Failure	3580 Volts	3500 Volts	3450 Volts	3405 Volts

1. Format the circuit and determine device power (P_d) for a series of input amplitudes (V_{EMP})

2. Manually plot P_d versus V_{EMP}

3. Locate V_{EMP} for $P_d = K_R t^{-1/2}$

The three codes used to demonstrate computer-aided damage threshold analyses have the capability of combining steps 1 and 2 above (i.e., to plot P_d as a function of V_{EMP} directly. Some attempts have been made to incorporate the junction burnout model into existing codes (References 14 and 15) but at this time evaluation of this approach is not complete. Considering the EMP analysis code development and device model development currently in progress, computer-aided damage analysis may become more practical and cost effective in the foreseeable future. The primary limitation to damage analyses in general is the limited component burnout data base.

6. REFERENCES

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3. Wunsch, D. C., and L. Marzitelli, "BDM Final Report Volume II, Semiconductor and Nonsemiconductor Damage Study," (Confidential), Contract No. DAAK02-67-C-0168, BDM Report BDM-374-69-F-0168, April 1969.

4. Wunsch, D. C., R. L. Cline, and G. R. Case, "Theoretical Estimates of Failure Levels of Selected Semiconductors Diodes and Transistors," Contracts F29601-69-C-0132 and F-29601-70-0019, BDM/A-42-69-R, December 1969.

5. Tasca, D. M., and J. C. Peden, "Pulsed Power Failure Modes in Semiconductor Devices," Conference Proceedings on Component Degradation from Transient Inputs, USAMERDC, April 1970.

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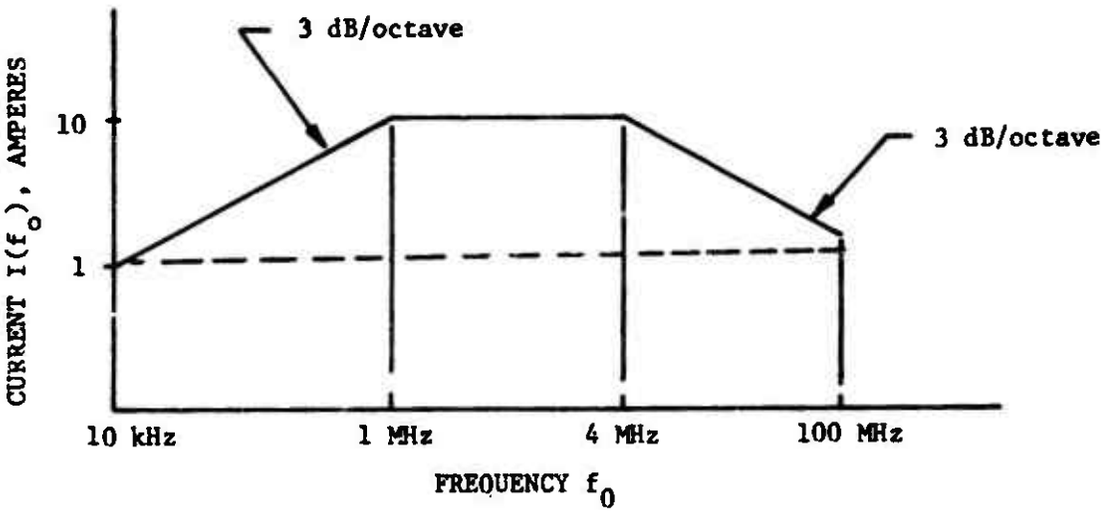
SECTION IV

EMP SOURCE CONFIGURATION ANALYSIS

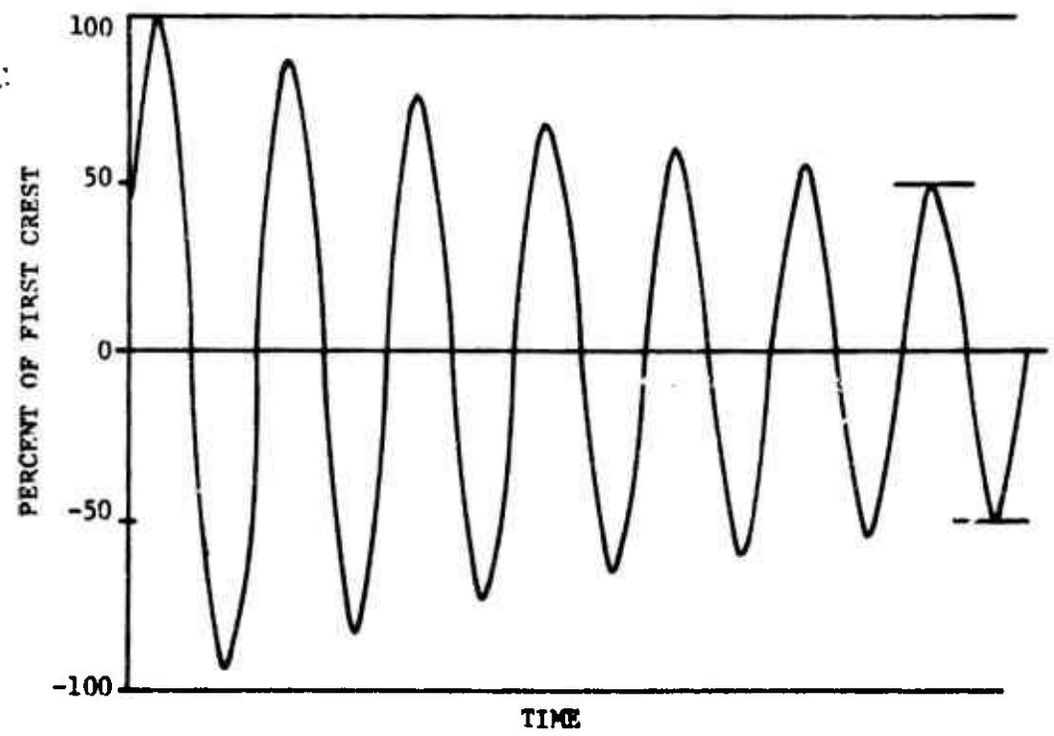
1. GENERAL

The performance of an EMP Susceptibility Threshold Analysis and Subsystem Vulnerability Assessment requires a definition of the EMP driving function and related source impedance. If an EMP specification has been derived for the system being analyzed, and if the subsystem cabling configuration is defined, the driving function and source impedance associated with each susceptible subsystem port may be computed using available approximation methods. The theoretical or experimental basis for defining a subsystem EMP specification is beyond the scope of this handbook and it is assumed that the circuit analyst is provided with either a common mode current or voltage specification applicable to the subsystem interfaces for which he is responsible. Such a specification has been defined for B-1 aircraft mission critical subsystems and is described in Figure IV-1. The current specified is the common mode current; that is, the algebraic sum of the currents in all of the cable conductors except the shield or ground plane. For the B-1, and most other aeronautical systems, the subsystem EMP environment is dependent on the subsystem location and configuration. Figure IV-1 actually represents a worst case composite common mode current specification which is applicable to all mission critical subsystems. Subsystems that are connected to antennas or are otherwise directly exposed to a free field environment are more difficult to analyze since the conducted interference levels must be defined before subsystem vulnerability analysis can commence. The coupling or energy capture analysis performed to determine conducted energy characteristics is beyond the scope of this handbook and the results of such studies are assumed to be available to impact hardware design and analysis.

Given a conducted interference specification and a specific cable configuration, this section describes and illustrates a number of approaches for generating EMP source configuration models (V_{oc}, Z_s) that can be used



(a) Peak Core Current Requirement for General Electronic Equipment



(b) Cable Core Current Waveshape

Figure IV-1. EMP Interference Test Specifications for B-1 Mission Critical Avionics

to asaess subsystem vulnerability. Since every subsystem interface connector and associated cable represents a special case deserving unique analytical consideration, the examples presented are intended as typical problems such as might be encountered in actual systems, not as general, universal illustrations.

2. SOURCE CONFIGURATION ANALYSIS

In the EMP frequency spectrum, the interface cabling associated with a given subsystem must generally be considered as a multiconductor transmission line. Transmission line analysis can be performed using either an exact coupled differential equation approach or an approximate lumped element multisection approach which approaches the exact solution as individual sections become infinitesimally short. A more detailed treatment of these two approaches can be found in References 1 through 5. Both of these methods require model descriptive data equivalent to short circuit impedances and open circuit admittances. Since the theory hss been trested in detail in the above references, only the advantages and limitations of theae methods will be discussed here.

The exact multiconductor transmission line method has the sdvsntage that a solution can be obtained independent of cable length. However, it is not as flexible as the lumped element section method for dealing with nonuniformities. Good estimates can be obtained by hand snalysis using the exact method on long one and two conductor cables while the lumped element approach would require a computer. The lumped element approach reduces to a circuit problem and has the advantage of schematically representing the interactive coupling occurring in multiconductor cables. Since the lumped element method reducea to solving a circuit problem, one of many computer codes can be used in either the time domain or the frequency domain. Codes svailable to the analyst include ECAP II, SCEPTRE, NET-2, and CIRCUS 2 (References 6 through 9). In addition, there are a number

of specialized codes which have been specifically developed for efficiently solving internal coupling problems. For example, TRAFFIC uses a frequency domain approach to analyze general N-conductor cables (Reference 10). Refereuces 11 and 12 describe other codes that analyze distributively excited multiconductor cables using exact multiconductor transmission line methods and which interface directly into TRAFFIC.

Even though the description of subsystem interface cabling is often complex, EMP vulnerability assessment often requires only worst case estimates of signal levels and it is acceptable to make approximations to simplify the analysis. Several useful approximations are discussed below and a few will be pointed out in the examples that follow.

The most frequencly used approximation in cable analysis is the concept of electrically short cables. This concept permits the use of simplifying assumptions if the cable length (ℓ) is much less than wavelength (λ) of the highest frequency of interest (i.e., $\ell \leq \frac{\lambda}{10}$). As pointed out in previous sections, many circuits are most vulnerable to low frequency energy which would permit the application of the electrically short approximations to physically long cables. Therefore, the cable response is determined primarily by the termination impedances. Given a subsystem EMP specification, this approach will yield an estimate of interface voltages or currents using a relatively unsophisticated analysis. Often hand analysis methods will be sufficient.

If a subsystem assessment involves one critical port, only two conductors of the cable need be considered in the analysis. In the case where EMP interface responses are being sought from a critical node to a reference, the conductors in the cable can be grouped to form a two conductor plus a reference transmission line problem. This model then can be solved using multiconductor transmission line theory. Two coupled second order differential equations are formed that can be transformed using eigenvalue-eigenvector techniques. Two uncoupled equations are then obtained that can be solved by standard ordinary differential equation

techniques (Reference 11). Often an additional approximation can be made neglecting all conductors in the cable except the one directly connected to the critical circuit of interest. In this case, the problem reduces to a single conductor plus a reference which results in a single second order differential equation that can be solved using ordinary differential equations (Reference 13). Some cables display a high degree of symmetry and for these cases a large reduction in analysis effort can be realized. In fact, many specific cases of this type require no more effort to solve than the two conductor case above (Reference 14). Approximations of the type discussed in this paragraph frequently reduce very large analysis problems to problems that can be worked with desk top calculators.

Along with understanding the cable system for which source characteristics are desired, one should know what form of interface connector source data are most useful. If the subsystem being investigated has nonlinear input characteristics or the source cable represents the drive for many different inputs, it would be advantageous to use an equivalent model of the cable such as a Thevenin equivalent (see Appendix E). Although, for those subsystems that have linear inputs where the interface cabling is not typical, it is most efficient to analyze the cable and subsystem input circuitry as one problem. For those cases, the signal levels on the critical input circuit elements are determined directly. The cable source information can be obtained in either of these forms using theoretical techniques or experimental techniques. In the case where the source characteristics are desired in terms of a Thevenin equivalent (or Norton equivalent), it is possible to obtain the equivalent from calculations, from measurements of the actual cable (or a similar one), or from references where a number of equivalent circuits have been tabulated

such as Appendix E. However, if a representative equivalent model is selected from a reference table, care should be taken to be sure the cable which was used to generate the equivalent model is indeed representative of the cable that is actually connected to the subsystem being analyzed.

The following examples are shown as an attempt to demonstrate a few of the above approaches to obtaining source characteristics. There are many variations of the described techniques and approaches that can be used by the analyst and the best approach would probably be the one with which he is most familiar. However, all the system data that are available should be used and as many variables as feasible should be included in the analysis. When possible, more than one approach should be taken to verify the model and associated approximations. The examples here appear in a sequence representing an increasing sophistication in the analysis processes.

a. Analysis of Electrically Short, Small Cables

In this example, an interface electronics unit will be considered for assessment to EMP damage. The interface specification used to assess the vulnerability of the circuit will be similar to the B-1 specification except it will specify a peak voltage instead of a peak current. The voltage amplitude will be 100 volts at 10 kHz and 1 kV at 1 MHz; the amplitude remains constant to 4 MHz and then rolls of at 3 dB/octave. The circuit is interfaced to an accelerometer drive unit by a 7 meter long shielded twisted pair as shown in Figure IV-2.

Circuit damage threshold is dependent on EMP frequency or equivalent pulse duration. The Wunsch Model (Section III) shows damage of semiconductor junctions to be inversely proportional to pulse duration, therefore the shorter pulse durstion (higher frequencies) are less significant in evaluating component damage than the longer pulses. Furthermore,

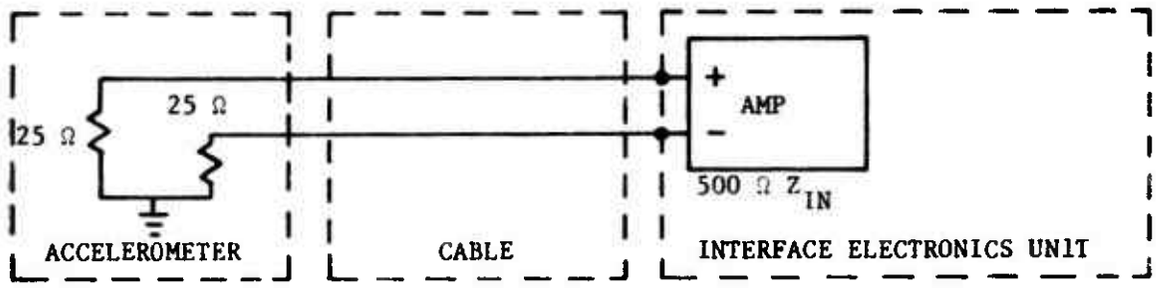


Figure IV-2. Interface Circuit and Cable

the specification flattens out at 1 MHz and rolls off at 4 MHz which makes it reasonable to assume that frequencies above 4 MHz can be ignored. Using the propagation velocity of light for the propagation of the EMP signal on the cable, the minimum wavelength that needs to be considered is

$$\lambda_{min} = \frac{c}{f_{max}} = \frac{3 \times 10^8}{4 \times 10^6} = 75 \text{ meters}$$

The cable in this case is much less than λ_{min} making it electrically short ($\leq \lambda$ min/10) and therefore, its characteristics can be represented by a single lumped element section. Assuming that the EMP signal is induced on the cable in series with the 25 ohm source terminations, the problem is illustrated by the circuit in Figure IV-3.

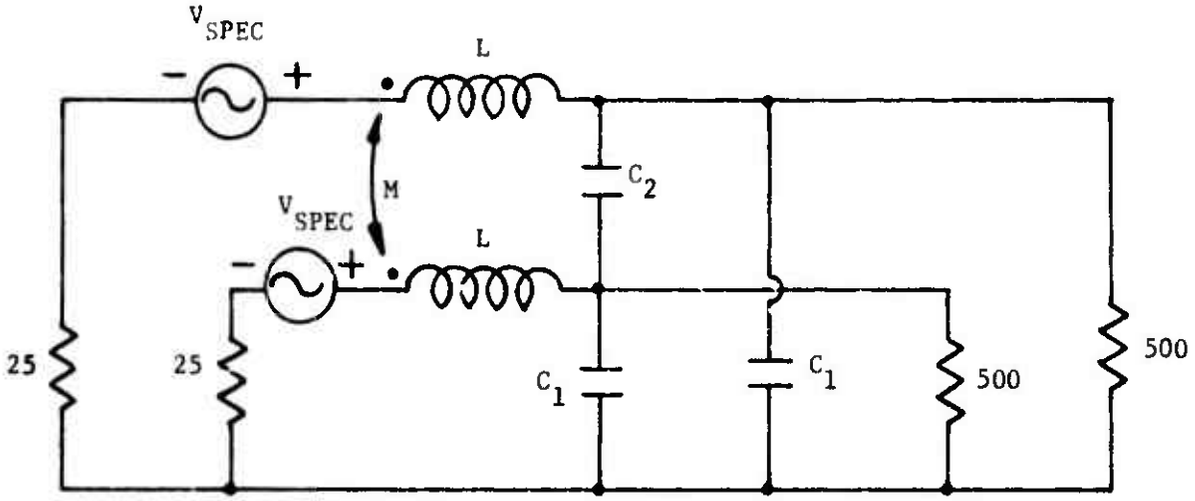


Figure IV-3. The Circuit Problem

The L, M, and C values in this circuit represent the per unit length parameters for this cable times the length of the cable. These per unit length parameters can be estimated by the standard logarithmic expressions as presented in References 15 and 16 or from tables and formulas in any appropriate engineering handbook. A more detailed discussion on evaluation of cable parameters can be found in Reference 17. For this example the following expressions were used to estimate the per unit length parameters.

$$L_i \simeq .2 \ln_e \frac{2D}{r} \text{ uh/m}$$

$$M_{ij} \simeq .2 \ln_e \frac{2D}{\overline{ij}} \text{ uh/m}$$

$$[L] \equiv \begin{bmatrix} L_1 & M_{12} \\ M_{21} & L_2 \end{bmatrix}$$

$$[K] = \frac{\varepsilon_d}{9 \times 10^{16}} [L]^{-1} = \begin{bmatrix} K_1 & K_{12} \\ K_{21} & K_2 \end{bmatrix}$$

$$C_{ij} = -K_{ij} \text{ pf/m}$$

$$C_{io} = K_i - \sum_{\substack{j=1 \\ j \neq i}}^{n} C_{ij} \text{ pf/m}$$

where $i, j = 1, 2$

L_i is the per meter self inductance of the i^{th} conductor, M_{ij} is the per meter mutual inductance between the i^{th} and j^{th} conductors, D is the distance of the center of the i^{th} conductor from the reference, r is the radius of the i^{th} conductor, $\overline{ij}$ is the center t_o center spacing between the i^{th} and j^{th} conductor, ε_d is the effective relative dielectric constant between the conductors and shield, [K] is the elastance matrix which is proportional

to the inverse of the [L] matrix, C_{ij} ia the per meter mutual capacitance between conductors i and j, and C_{io} is the per meter capacitance between only the i^{th} conductor and the reference.

For this example the per unit length parameters were calculated aa

$$C_{10} = C_{20} = 54 \text{ pf/meter}$$

$$C_{12} = 32 \text{ pf/meter}$$

$$L_1 = L_2 = .27 \text{ uh/meter}$$

$$M_{12} = .1 \text{ uh/meter}$$

The wire radius used was for AWG #20 gauge wire with a 2.9 relative dielectric conatant insulation. The tranamiasion line loaaea are amall and were assumed to be negligible. Using the above values the cable circuit values can be calculated aa:

$$L = 1.9 \text{ uh}$$
$$M = .7 \text{ uh}$$
$$C_1 = 380 \text{ pf}$$
$$C_2 = 225 \text{ pf}$$

The voltage across the 500 ohm reaiator ia required for the damage aaaess-ment. Upon examination of the circuit, it can be seen that the circuit is balanced and there will not be any potential developed acroaa C_2. Thia indicatea the currenta are equal in both conductora; therefore, the circuit equations can be written in the frequency domain aa

$$(25 + j\omega L + j\omega M + Z)\ I = V_{apec}$$

where I is the current in either of the conductors and $Z = 500/(1/j\omega C_1)$. The required voltage can then be solved for as

$$V = \frac{10^{15} \times V_{spec}}{(j\omega)^2 + 1.5 \times 10^7 \ (j\omega) + 1.0 \times 10^{15}}$$

and plotted as shown in Figure IV-4.

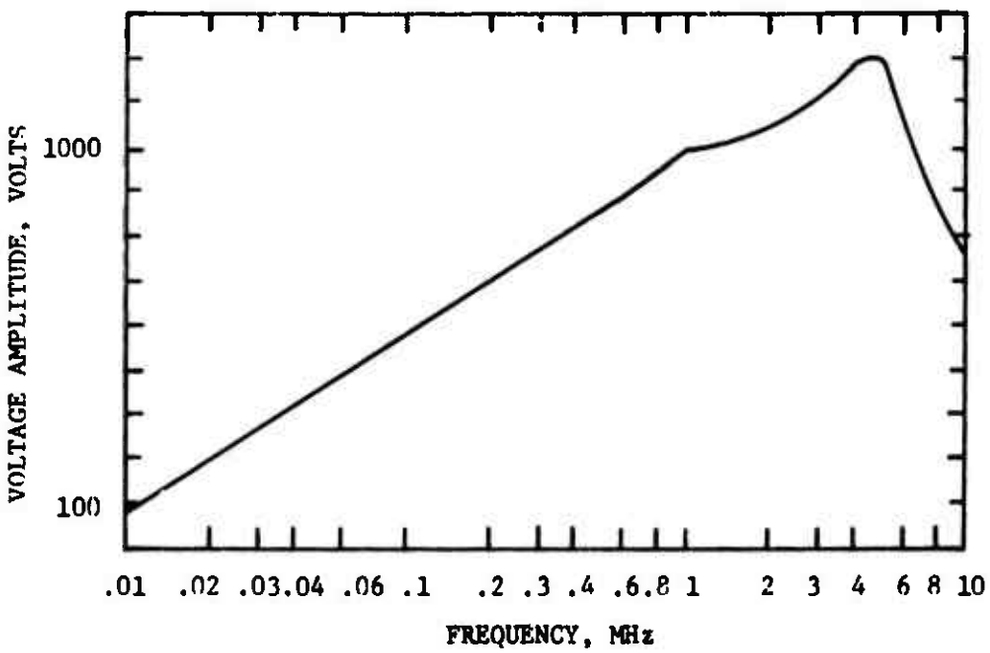


Figure IV-4. Subsystem Interface Voltage

In this analysis the time domain response resulting from the damped sine wave common mode voltage excitation will be sssumed to look similar to the excitation signal. This is only true in theory if the excitation is sinusoidal or if the frequency response of the network over the fraquency spectrum of the excitation signal is flat. In this case the damped sine wave excitation has a very low damping coefficient and therefore the frequency spectrum of this excitation contains most of its energy at the particular resonant frequency of the excitation. Therefore the frequency response data as it appears in Figure IV-4 will be used to predict the peak

damped sine wave response signal resulting from the excitation at a particular frequency as defined by the B-1 specification in Figure IV-1. The assessment can then be accomplished using these data with subsystem damage threshold information.

b. Two Wire Analysis of Electrically Short, Large Cables

For this example, an automatic control system, stability augmentation unit, is to be assessed for EMP damage. In particular, the aft accelerometer input is to be considered. The B-1 specification applied to the accelerometer end of the cable will be used to assess the subsystem. The cable considered here is a 5 meter 14 conductor bundle mounted along the inside structure of the fuselage. The circuit and cable are described in Figure IV-5.

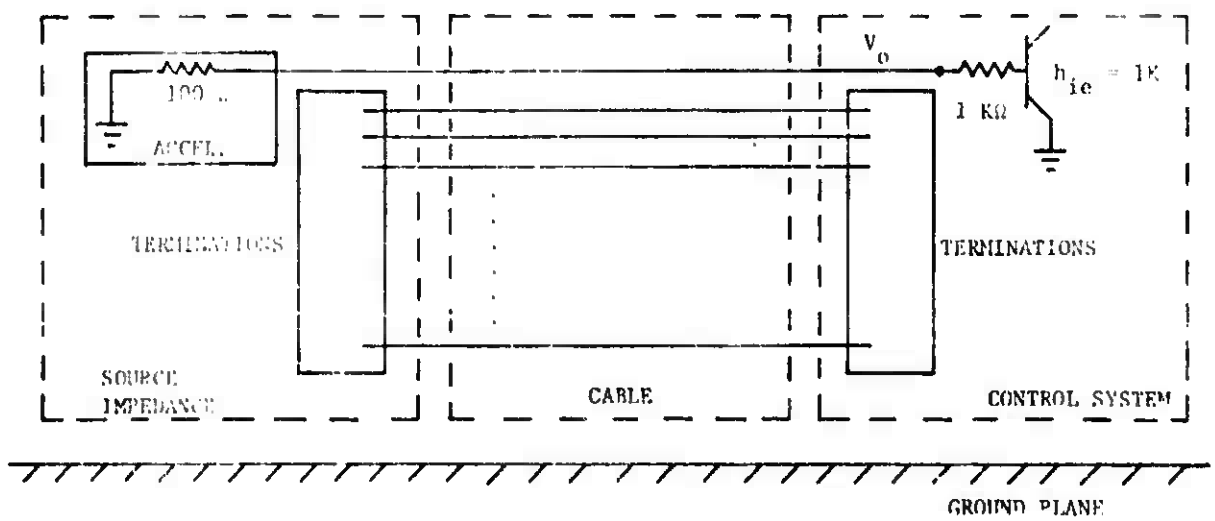


Figure IV-5. Interface Circuits and Cables

This problem will be approached by grouping the 13 conductors not directly connected to the circuitry of interest and considering then as one conductor. This effectively reduces the cable from a 14 conductor cable to a two conductor cable. Each termination, source and load, for the 13 conductor group is computed using common mode cable analysis techniques which define the equivalent termination to be the parallel equivalent of all the individual impedances tied together (Reference 13). The cable with terminations can now be shown as drawn in Figure IV-6.

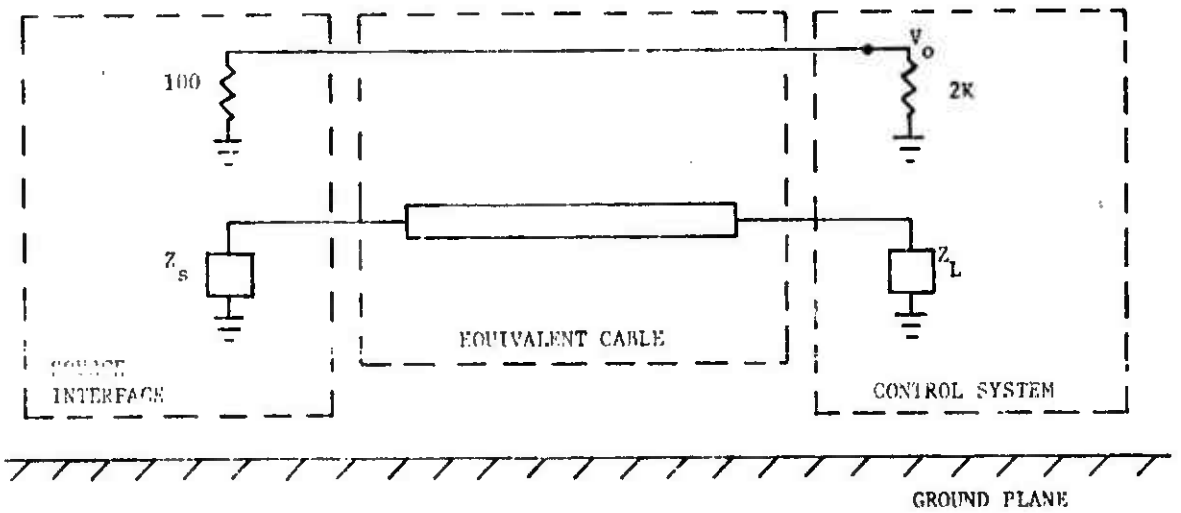


Figure IV-6. Circuit and Cable Equivalent Circuit

Most large cable bundles will have at least one individual wire termination that is a very low impedance or a ground. This means the common mode impedance as defined will be small or zero. However, recent studies have shown that there is a lower impedance limit for frequencies above a few hundred kHz. This lower limit is approximately 20 ohm and is due to the mutual coupling to other higher impedance lines (Reference 13). For this problem, 20 ohms will be assumed for Z_s and Z_L and these values will be examined for validity at the lower frequencies later.

As stated previously, the EMP excitation will be defined by the B-1 common mode cable current specification applied at the source interface. The current is generally considered to be induced on the cable by mutually induced series voltages in each of the conductors. For the purpose of simplicity, the induced voltages on the individual conductors are all assumed to be equal. It is then necessary to compute the value of this voltage as related to the B-1 current. This voltage can be estimated by using the total common mode impedance as seen by the B-1 common mode current on the cable. Using the approximate total common mode impedance of 40 ohms and the B-1 common mode current, the induced voltages sought will be estimated as 40 times the B-1 current.

To complete the circuit description so an assessment can be made, the cable parameters must be estimated for the "two wire" cable model. As discussed in example (a), damage threshold is inversely proportional to the pulse duration; therefore, the high frequency components of the pulse will be ignored and the analysis will be conducted for frequencies below 5 MHz. Using a maximum frequency of 5 MHz and a signal propagation equal to the velocity of light, the minimum wavelength on the line is computed as 60 meters, therefore the line is electrically short. The cable will be modeled by one lumped element section. The cable and interface circuitry can then be described by a circuit as shown in Figure IV-7.

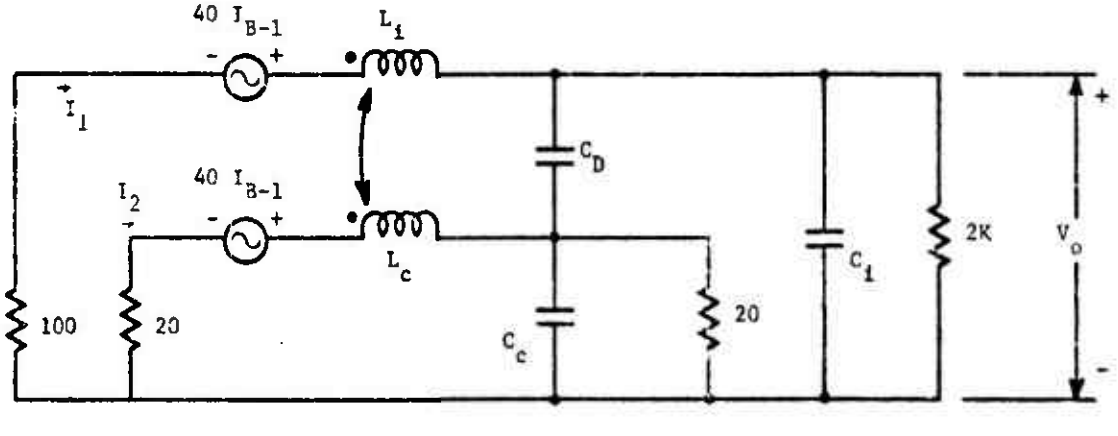


Figure IV-7. Circuit Model

The per unit parameters must be computed to obtain the circuit values representing the cable section. As indicated in the previous example, these parameters can be estimated using standard handbook expreasions. Using per meter parameters and s five meter length the following circuit values were defined.

$$M = 3.3 \text{ uh}$$
$$L_i = 5.2 \text{ uh}$$
$$L_c = 3.45 \text{ uh}$$
$$C_d = 367.5 \text{ pf}$$
$$C_c = 75 \text{ pf}$$
$$C_i = 6 \text{ pf}$$

Either hand snalysis of computer analysis can now be used to obtain the exact voltsge, V_o, in terms of the other circuit elements. As an aid to understanding current and voltage distributions on a cable, the solution will be obtsined by using hand analysis.

The impedance represented by C_c is much larger than 20 ohms for the entire frequency range of interest and therefore will be neglected. Also, the capacitance C_i is very small and its impedance to ground will also be neglected. The 13 conductor bundle represented by the lower part of the circuit is terminated with small 20 ohm impedsnces while the conductor of interest is s high impcdance circuit. For dc conditions, the current I_2 is approximately 50 times the current I_1. Since

$$I_1 X_m << I_2 X_m$$

the voltage induced on 13 conductor bundle may be neglected. Therefore the current I_2 may be solved for independently and then used to solve for I_1. Once these currents are found, the above assumptions will be verified and, if necesaary, the solution will be iterated to improve the accuracy. Using these sssumptions s solution can now be obtained using hand analysis.

$$I_2 = \frac{I_{B-1}}{8.63 \times 10^{-8} (j\omega) + 1}$$

This expression shows I_2 as being independent of I_1 and indicates that I_2 rolls off at 3 dB/octave above 1.85 MHz. Using the assumption $I_2 = 50\ I_1$, V_o can be written as

$$V_o = \frac{Z_e\ 40\ I_{B-1}}{100+j\omega L_i+j\omega 50M+Z_e}$$

where

$$Z_e = 2K//(50 \times 20 + \frac{1}{j\omega C_D})$$

Using the appropriate circuit values, the above expression reduces to

$$V_o = \frac{.953\ (3.675\times10^{-7}\ (j\omega) + 1)\ 40\ I_{B-1}}{8.94\times10^{-14}(j\omega)^2 + 4.84\times10^{-7}(j\omega) +1}$$

This can be plotted as shown in Figure IV-8.

Current I_1 may be expressed as

$$I_1 = \frac{\frac{1}{52.5}\ (1.1 \times 10^{-6}\ (j\omega) + 1)\ I_{B-1}}{8.94 \times 10^{-14}\ (j\omega)^2 + 4.84 \times 10^{-7}\ (j\omega) + 1}$$

Upon close examination it was found that I_1 is approximately 50 times smaller than I_2 over the entire frequency range of interest. Therefore, the calculated voltage will be assumed accurate and will be used for the subsystem damage assessment.

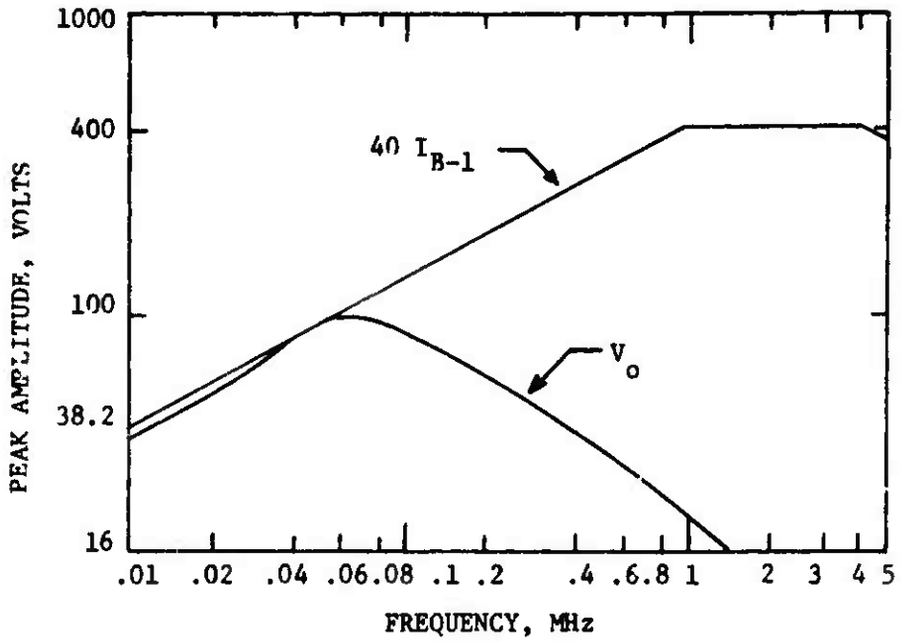


Figure IV-8. Interface Voltage at Subsystem

For frequencies below a few hundred kHz the mutual coupling to high impedance lines will be minimal and lead inductance will produce a very small impedance. Therefore the common mode impedance will be smaller than the 20 ohms assumed earlier. Using a lower impedance for low frequencies, nearly all the common mode current will be traveling down the large 13 conductor bundle and very little will appear on the conductor of interest. This will tend to reduce the voltage level (V_o) at low frequencies and is therefore not the worst case.

This example demonstrated the two wire approach on a cable that was electrically short. With a little additional effort, longer cables can be analyzed. The number of lumped element sections required for a longer cable will be approximately $\ell/.1\lambda_{min}$, where ℓ is the physical cable length and λ_{min} is the smallest wavelength to be considered. The additional complexity of the model may require the use of a computer aided technique.

c. Single Line Analysis of a Long, Large, Complex Cable

This example involves the upset hardening of an Inertial Navigation System. The common mode voltage shown in Figure IV-9 is specified. The cable with representative source and load terminations and the particular circuitry being assessed is shown in Figure IV-10.

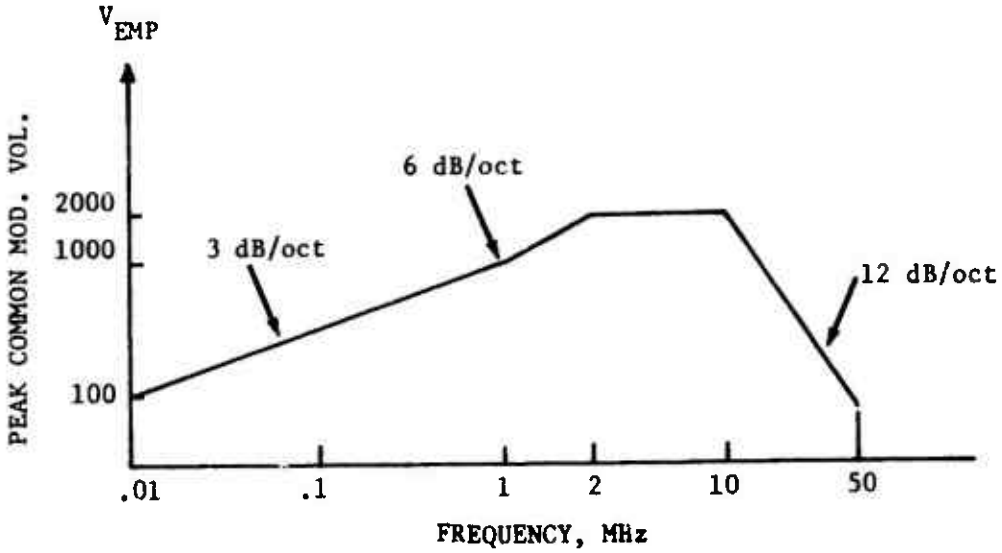


Figure IV-9. Measured Common Mode Excitation

The circuit of interest here is the 1K ohm source driven conductor with the 10K ohm operational amplifier load. A rigorous approach to this problem would require a full N wire model of the cable system representing the many differentially coupled TEM modes that actually exist on the cable. This approach, however, would require the use of a computer code and large computer. An approximate approach will be taken that will allow the solution to be obtained using a desk-top calculator.

The approach used is shown in Figure IV-11 and consists of modeling the one conductor associated with the critical circuit as though coupling to the rest of the conductors in the cable existed only at the terminations.

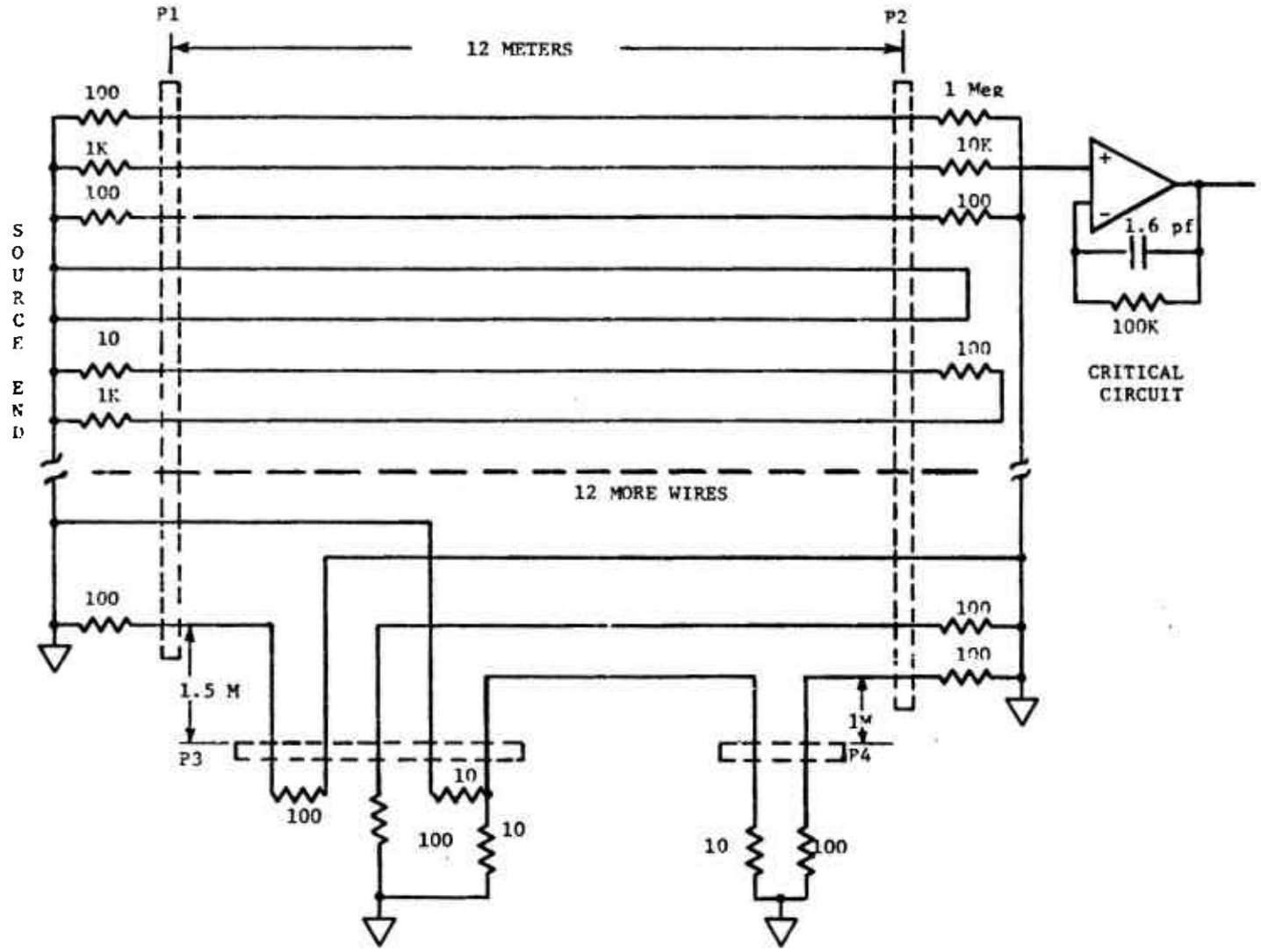


Figure IV-10. Cable and Circuit Configuration

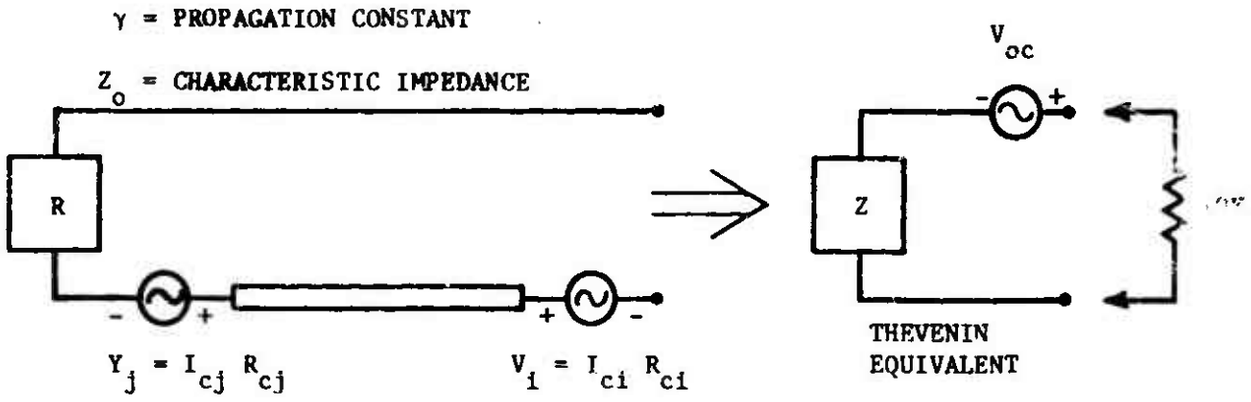


Figure IV-11. Single Line Model for Individual Wire

A Thevenin Equivalent is desired for this model from estimated values of γ, Z_c, V_j, and V_i. With the use of transmission line impedance expressions and the approximate induced voltages at the cable ends, the values for the Thevenin Equivalent can be computed. Since this analysis was made on a desk-top calculator, only the equations and the results will be shown.

The first problem is to compute the Thevenin impedance for the conductor associated with the critical circuit. If the wire of interest can be represented by a single uniform transmission line, then the impedance can be expressed in terms of standard transmission line equations. One convenient form is

$$Z_{TH} = Z_o \frac{Z_L \text{ Cosh } \gamma\ell + Z_o \text{ Sinh } \gamma\ell}{Z_L \text{ Sinh } \gamma\ell + Z_o \text{ Cosh } \gamma\ell}$$

where, Z_o is the characteristic impedance of the line, γ is the complex propagation constant of the line, ℓ is the length of the line, and Z_L is the load impedance on the line. The length is chosen to be equal to the

actual length of the particular wire of interest which for this example is 12 meters. The load impedance is taken to be the actual source end impedance to ground which for this case is 1K ohm.

For shielded cables, all TEM modes of propagation will have nearly the same propagation properties. Unshielded cable bundles, over a ground plane, will have at least one mode, for example the common mode, that will have a significantly different propagation characteristic. This cable is unshielded and is mounted along the inside of the fuselage approximately two inches above the structure and, therefore, demonstrates a common mode propagation property quite different from that of the differential modes. However, for this single line mode, the constants Z_o and γ will be chosen based on differential mode propagation properties. Differential mode properties are applicable because one or more wires will be grounded or have a low impedance to ground at both ends of the cable. The cable impedance will therefore be high between the ground wire and the other wires in the cable. Thus, it is conjectured that the differential mode determines the propagation properties. The velocity of propagation is thus related to the free space velocity of light by the effective relative dielectric constant of the insulation around the wires. Assuming the individual wire propagation losses to be negligible the propagation constant can be written as

$$\gamma \simeq j\beta = j \frac{2\pi f_M}{300} \sqrt{\epsilon_d}$$

where f_M is frequency in MHz and ϵ_d is the dielectric constant (assumed 2.3).

The characteristic impedsnce, Z_o, will have a value between the impedance of two adjacent parallel wires in the cable and a coaxial line where all other wires in the cable act like the outer coax conductor. For the calculations in this example, 100 ohms will be chosen for Z_o.

Measurements of several similar cables show this to be a reasonable value (Reference 13). Using the above propagation constants, the Thevenin impedance (Z_{TH}) was calculated from the above expression and plotted as shown in Figure IV-12.

In order to calculate the induced voltages V_i and V_j at the ends of the single wire model, a simple model for the common mode current must first be generated. This model will then be used to approximate the common mode currents at the terminations due to the excitation at the source end of the cable. The model used is described by a single line representing the cable bundle as one conductor over the ground plane. A schematic diagram for this is shown in Figure IV-13.

Each segment of the cable from a termination to a branch or between branches must be modeled as one section of the total common mode model. The sections will be modeled using standard transmission line impedance expressions and will be described by a cascade two port network representation as shown in Figure IV-14.

The cascade parameters can be written as:

$$A = D = \text{Cosh } \gamma_c K$$

$$B = Z_c \text{ Sinh } \gamma_c K$$

$$C = \frac{1}{Z_c} \text{ Sinh } \gamma_c K$$

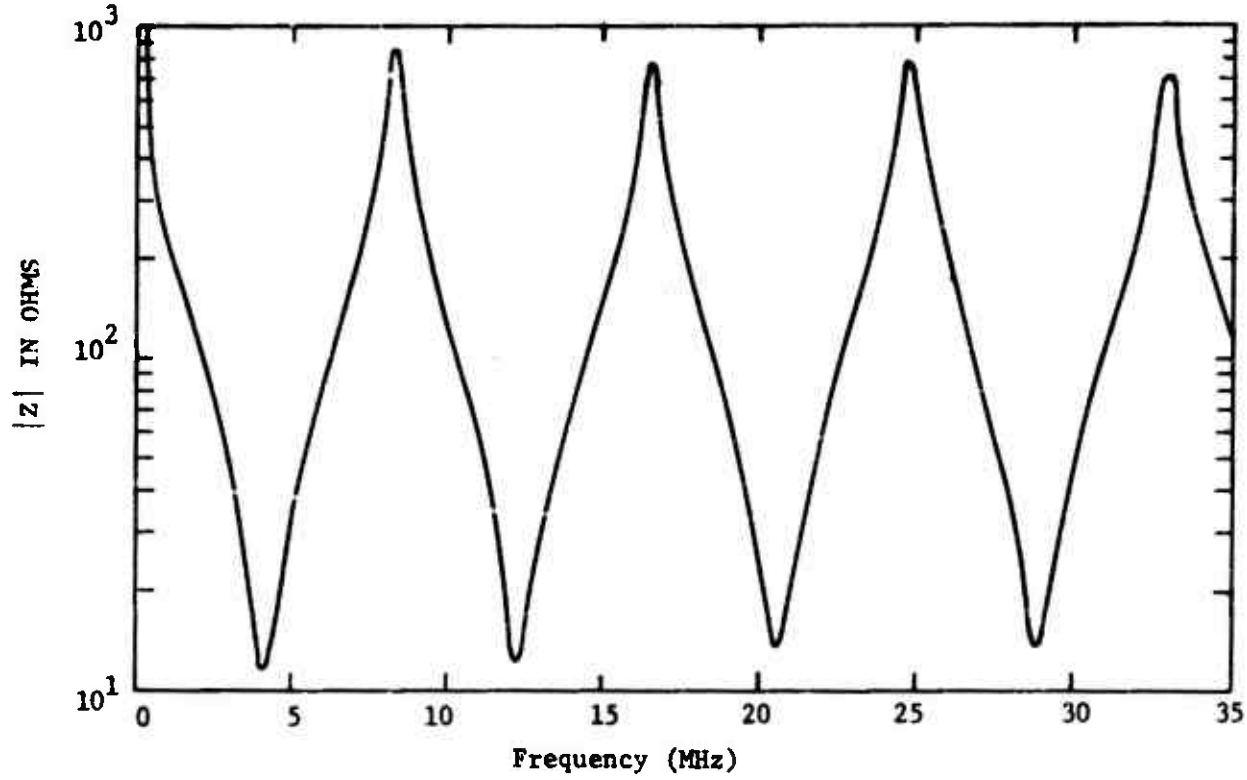


Figure IV-12. Thevenin Equivalent Circuit Impedance

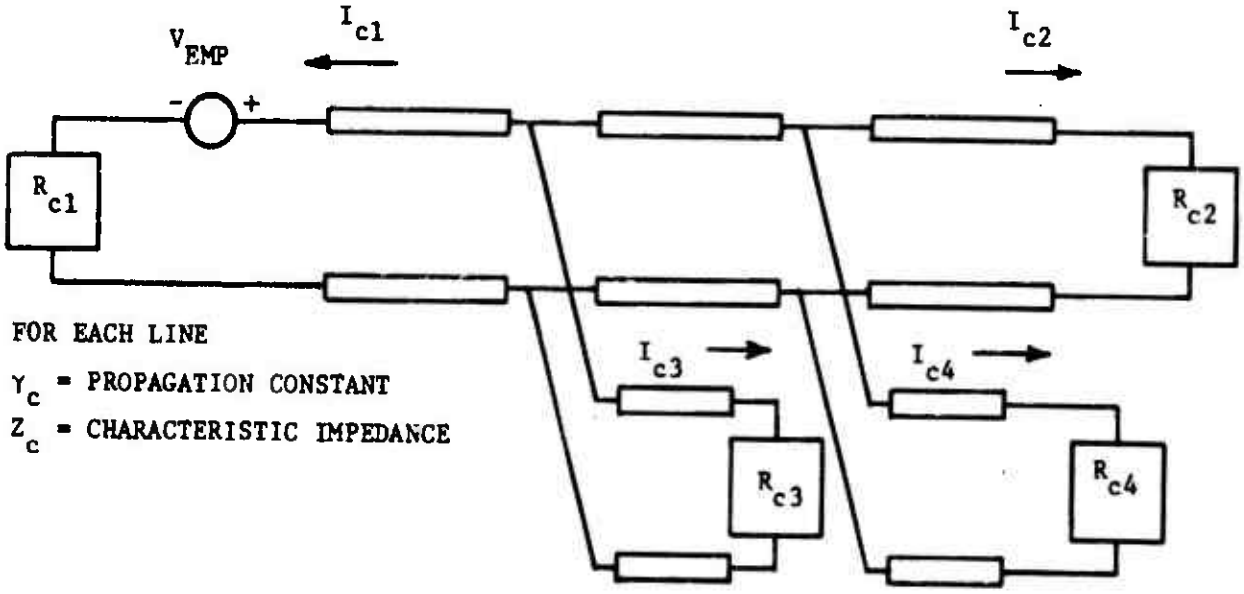
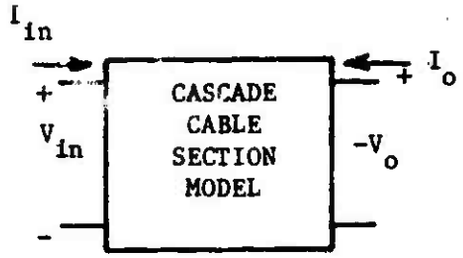


Figure IV-13. Single Line Common Mode Model



$$\begin{bmatrix} V_{in} \\ I_{in} \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_o \\ -I_o \end{bmatrix}$$

Figure IV-14. Common Mode Model of Cable Section

Where Z_c is the common mode characteristic impedance of the cable segment, γ_c is the common mode propagation constant of the cable segment, and K is the length of the cable segment. The constants γ_c and Z_c can be computed from the per unit length common mode parameters using the expressions

$$\gamma_c = \sqrt{Z_{cm} Y_{cm}} \cong j \frac{2\pi f_M}{300} \sqrt{\varepsilon_c}$$

$$Z_c = \sqrt{\frac{Z_{cm}}{Y_{cm}}} \cong \sqrt{\frac{L_c}{C_c}}$$

Where f_M is frequency in MHz and ε_c is the effective relative dielectric constant between the cable bundle and the reference. For the unshielded bundle over ground plane in this example, ε_c is assumed to be one, but for a shielded cable it will be nearly equal to the relative dielectric constant of the insulation. The common mode per unit length parameters for this bundle over ground plane can be estimated as

$$L_c = .2 \ln_e \frac{2h}{R} \text{ uh/meter}$$

$$C_C = \frac{\varepsilon_c}{9L_c \times 10^4} \text{ pf/meter}$$

where h is the height of the cable center above the ground plane and R is the cable radius.

The cascade networks and common mode loads along with the EMP common mode excitation voltage can now be used to calculate the voltages V_j and V_j. It is assumed that the voltage csused by the common mode current across the common mode loads is a series voltage at each end of the single line model for the individual wire. It is also assumed here that the common mode impedance for this cable will differ very little from 20 ohms, therefore, 20 ohms will be used. The common mode currents I_{c1} and I_{c2} in Figure IV-13 must be determined so V_j and V_i can be obtained. All common mode currents in this cable will be dependent on the EMP excitation voltsge which was shown in Figure IV-9.

By using current dividing expressions involving common mode admittances, the currents I_{c1} and I_{c2} can be computed. Starting from the right side of the diagram in Figure IV-13, the admittance at the branch looking toward R_{c2} can be computed as

$$Y = \frac{C + AY_L}{A + BY_L}$$

where A, B, and C are the common mode cascade psrameters for the section of cable loaded by R_{c2} and Y_1 is the load I^1/R_{c2}). This is done also for the section of cable losded by R_{c4}. These two computed admittances in parallel (slgebraicslly summed) become the load on the cable section between the brsnches. Proceeding to the source, the current I_{c1} can be computed and then divided at the first branch. After repesting this for the second branch, I_{c2} can be found. The voltages V_j and V_i now simply become $20I_{c1}$ and $20I_{c2}$ respectively. The Thevenin open-circuit voltage can subsequently be written in terms of a standard transmission line equation for the single line model shown in Figure IV-11. One convenient expression in the notation of Figure IV-11 is:

$$V_{oc} = \frac{-V_i}{\frac{R}{Z_o} \text{Sinh } \gamma\ell + \text{Cosh } \gamma\ell} + V_i$$

Using this expression and an HP 9820 desk-top calculator with a plotter, the following plot was made as shown in Figure IV-15.

The Thevenin equivalent circuit is described by the Thevenin impedance magnitude (Figure IV-12) and Thevenin voltage magnitude (Figure IV-15) and can be used to make estimates of the voltage and current signals seen by the critical circuit. The circuit input impedance (10K ohm) is large compared to the Thevenin circuit impedance (1K ohm max), therefore, the voltage seen at the critical circuit will be approximately the Thevenin voltage. Assessment can now be made of the vulnerability of the circuit and if hardening is necessary, the analysis can easily be repeated with the added hardening devices using the Thevenin equivalent circuit for the cable source characteristics.

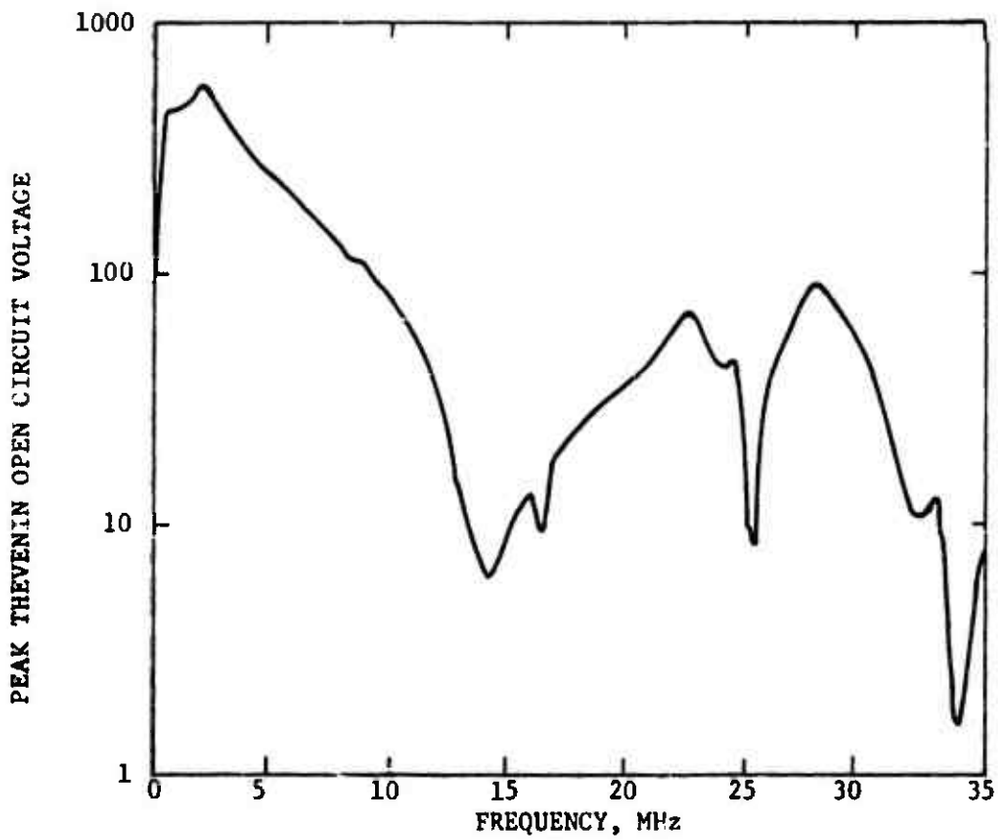


Figure IV-15. Thevenin Voltage Magnitude

d. Computer Analysis of Long, Large Cables

This example is drawn from the upset hardening of a digital accumulator in an Inertial Navigation System. The B-1 common mode current is applied at the source end of the cable as shown in Figure IV-16. The cable involved is 32 feet long and consists of a 49 conductor bundle mounted approximately two inches above the ground plane (aircraft fuselage).

In this example, the current source is inserted between the source terminations and ground. The cable common mode current can therefore be forced down the cable independent of frequency-dependent impedances.

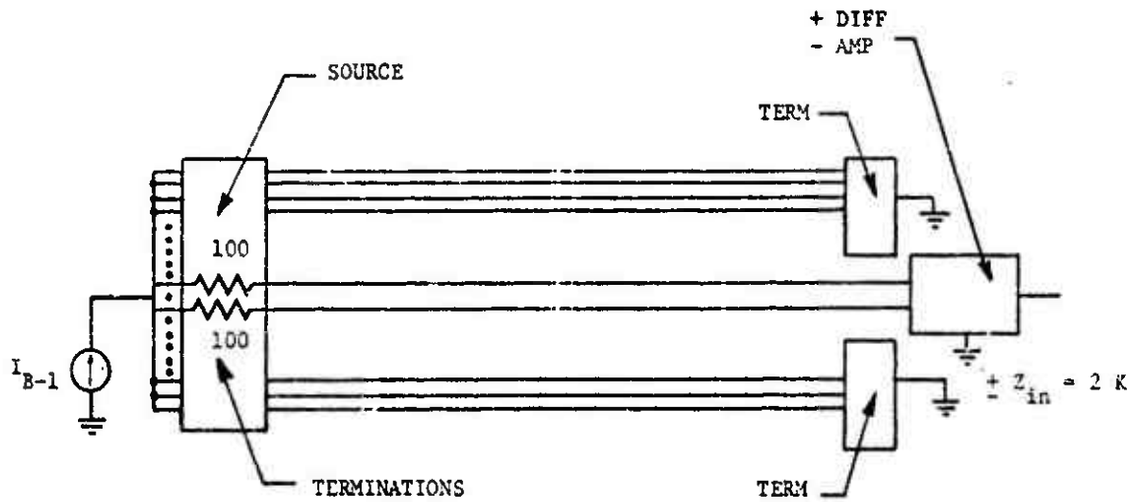


Figure IV-16. 49 Conductor Cable and Terminations

The termination for both ends of the critical subsystem was chosen to be random resistive loads between 1 ohm and 10K ohms.

Lumped element section modeling was used to obtain the voltages at the differential amplifier input. An attempt was made here to include as much detail in this 49 conductor model as was feasible. This process was accomplished using a large computer and computer code as described below.

The actual cable analysis was accomplished using the code TRAFFIC (Reference 10). Since the lumped element section model was used, it was necessary to determine the number of sections required and the per unit length cable parameters which define the elements in each section. First, the number of sections required was estimated by specifying the upper frequency to be used in the analysis. For this analysis, the entire frequency range (10 kHz - 100 MHz) of the B-1 specification was used. To satisfy the criteria that each section be significantly less than the shortest wavelength of interest, 32 one-foot sections were used. Second, the cable parameters were supplied by the code GEOPRM1 (Reference 17). This code computes the per unit length self inductance, mutual inductance, capacitances and series losses of the cables and outputs the data on punched cards or magnetic tape which is then input to TRAFFIC. GEOPRM1 determines the parameters using logarithmic expressions for the geometric properties of the cable such as cable radius, spacing above the ground plane, conductor radius and number of conductors. However, if measured cable capacitance parameters are available, the program PRAM can be used to compute the per unit length cable parameters for direct input to TRAFFIC (Reference 18). GEOPRM1 and PRAM can also handle various cable geometries ranging from highly symmetric lay cables to complete random lay cables. In this case, the bundle was assumed to display a somewhat random conductor lay. The series losses are assumed to be proportional to the square root of the frequency.

After the initial vulnerability assessment was made on this subsystem, upset was evident and a filter was devised to harden the subsystem. The frequency properties of the filter is also plotted in Figure IV-17. The results obtained in this assessment are shown in Figure IV-18.

The results of the TRAFFIC cable analysis utilizing a one amp current source were modified to reflect the variation in the common mode current source as a function of frequency as shown in Figure IV-1. In addition, some experimental data were utilized to interpret the computer analysis data so that the results might compare to actual cable measurement data. In particular, a twisted pair in a cable bundle will display a differential to common mode signal attenuation ratio as shown in Figure IV-17 when the cable is driven common mode.

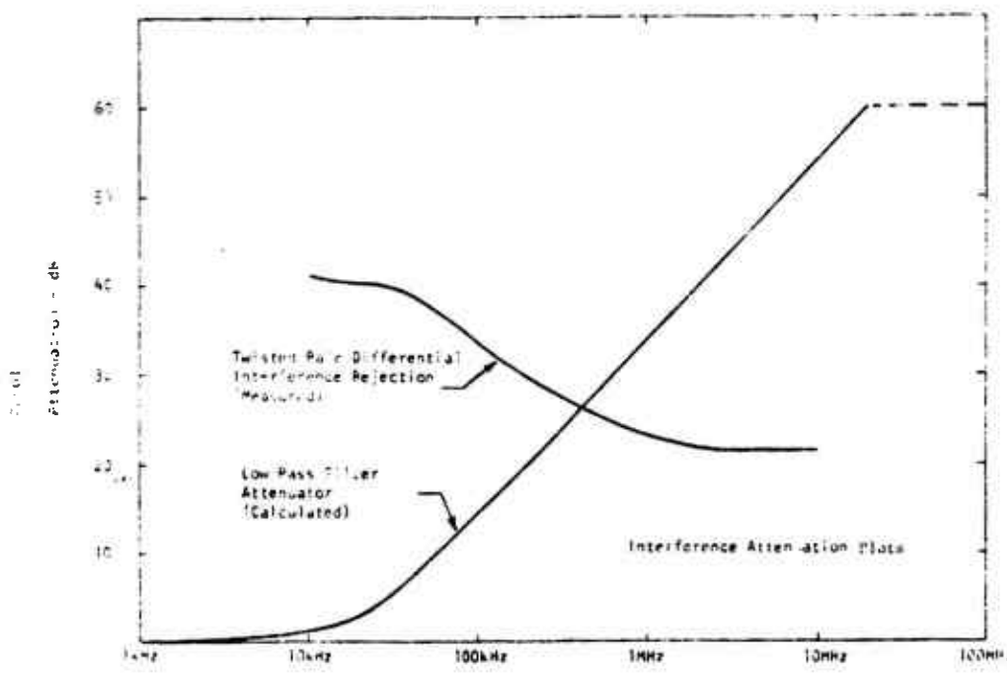


Figure IV-17. Spectral Responses

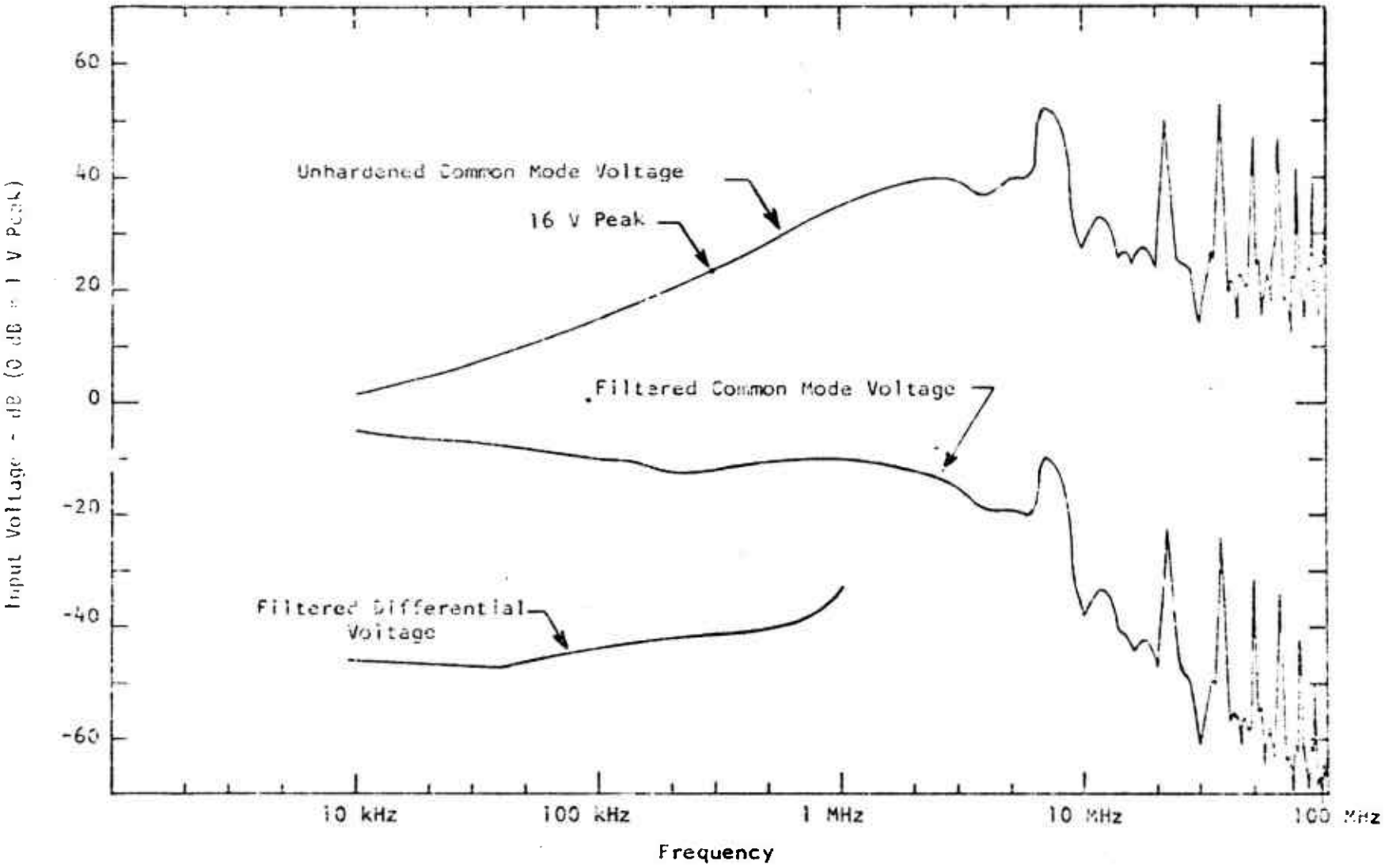


Figure IV-18. Critical Circuit Input Voltage from EMP

The common mode voltage seen on each conductor at the differential amplifier with respect to ground and the differential voltage between the terminals at the differential amplifier wa: necessary for proper assessment of this subsystem. Other signals and/or transfer functions are also readily available from this computer analysis.

In this analysis, the time domain response resulting from the damped sine wave B-1 common mode current excitation will be assumed to also look similar to the excitation signal. This is only true in theory if the excitation is sinusoidal or if the frequency response of the network over the frequency spectrum of the excitation signal is flat. In this case, the damped sine wave excitation has a very low damping coefficient and therefore the frequency spectrum of this excitation contains most of its energy at the particular resonant frequency of the excitation. Therefore, the frequency response data as it appears in Figure IV-19 predicts the peak damped sine wave response signal resulting from the damped sine wave excitation at a particular frequency as defined by the B-1 specification in Figure IV-2.

In practice, the effect of the cable network on the shape of the damped sine wave excitation may be required if a high degree of accuracy is desired. This can be accomplished by transforming the damped sine wave into the frequency domain by Fourier Trsnsforms, multiplying this frequency function times the transfer function of the cable system, and then transforming the frequency domain response voltage bsck into the time domain using inverse Fourier Transform routines. This technology is available in automatic data handling and computer program computations form (Reference 19).

In additica to frequency-time domain transformations and vise versa, it may be required to generate K port equivslent circuits. These will be necessary if nonlinesr subsystem analysis is required or if many cable system networks are to be connected. A discussion of K-port equivalent

circuit theory with examples is given in Appendix E. These techniques are also available using automatic computational techniques including rational polynomial admittance fitting for interface to CIRCUS 2.

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(16) Terman, F. E., "Radio Engineers Handbook," McGraw-Hill, 1943.

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(18) Spies, G. E., "In-Place EMP Integration Analysis," Boeing Document D2-19695-3, August 1971.

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APPENDIX A
SEMICONDUCTOR DEVICE MODELS FOR HAND AND COMPUTER ANALYSIS

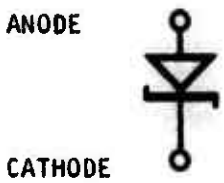
The analysis of circuits for upset or damage requires that models for the semiconductor devices be used. The choice of a model will depend on the type of analysis and the desired degree of accuracy. For example, hand analysis of a simple flip-flop for upset may require only a piecewise linear model of the diodes and transistors, whereas the same analysis done on a computer would require the Ebers-Moll model. The following sections present a discussion of some models that can be used for hand and computer analysis. In many cases the models for upset and damage will basically be the same. Differences that arise in using the models for either upset or damage will be pointed out.

1.1 HAND ANALYSIS MODELS

The piecewise linear model of the silicon Zener diode shown in Figure A-1 is used as the basic building block for establishing an approximate large signal, piecewise linear model for the silicon junction bipolar transistor.

As illustrated in Figure A-1, the actual i-v characteristics of a Zener diode are approximated by three broken-line segments. The reverse resistance r_r is shown as always being in the equivalent circuit but its effect is neglected since r_r is much larger than r_f and r_z. The D_d-V_d-r_f branch is in the circuit when the anode-cathode voltage exceeds V_d; whereas, D_z-V_z-r_z branch is in the circuit if the anode-cathode voltage is more negative than $-V_z$. Thus, the piecewise linear model with breakpoints at V_d and $-V_z$ allows complete delineation of the Zener diode modes of operation.

In practice, it is usually obvious which mode of operation exists (that is, forward biased, reverse biased, or reverse breakdown); however, if the mode of operation is not readily observed, one can simply assume the most likely mode of operation and use the appropriate equivalent circuit (Figure A-2)



ZENER DIODE

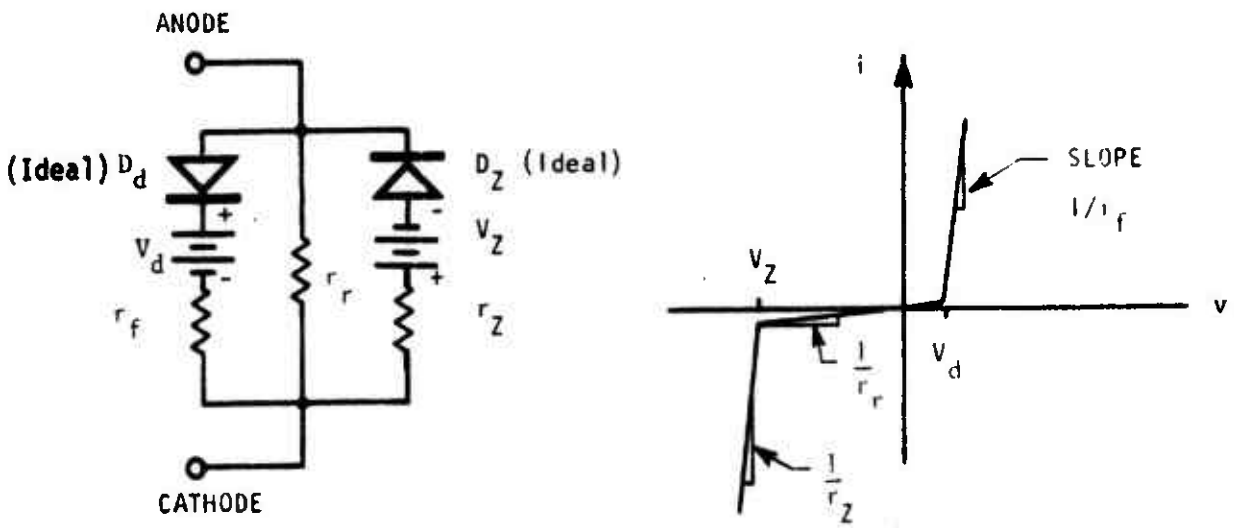
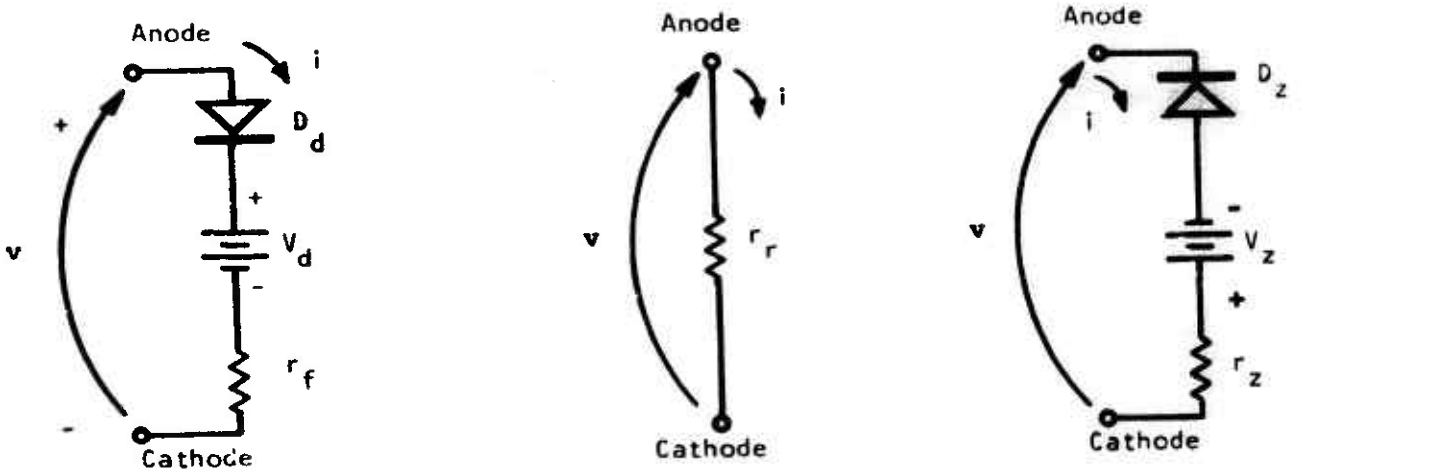


Figure A-1. Piece-wise Linear Model of Zener Diode and Corresponding i-v Characteristic



(a) Forward-Biased Equivalent Circuit; v > Vd, i only +.

(b) Reverse-Biased Equivalent Circuit; -Vz < v < Vd, i either + or -.

(c) Reverse-Breakdown Equivalent Circuit; v < - Vz, i only -.

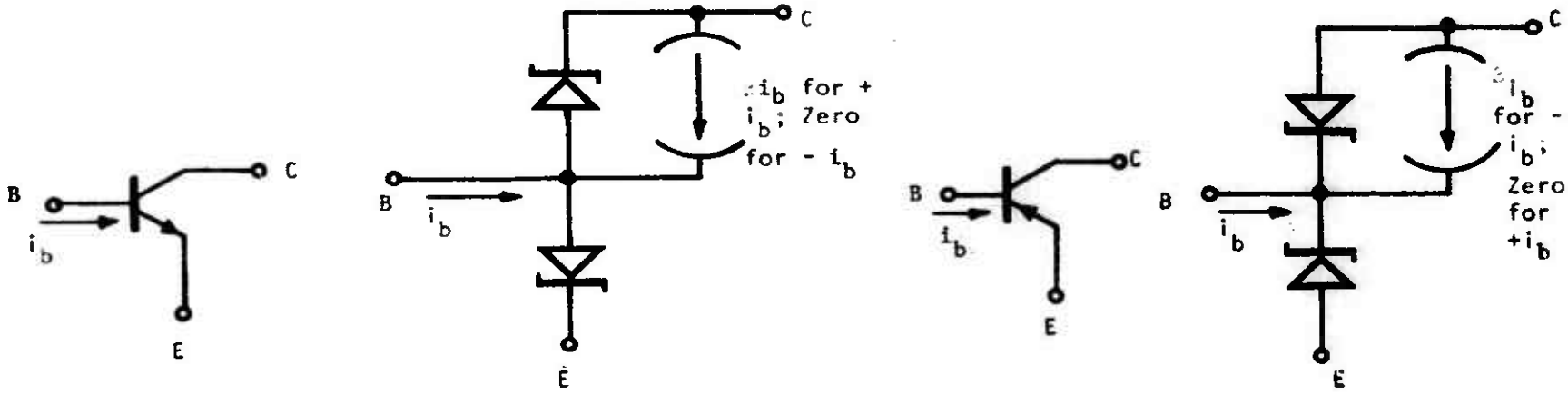
Figure A-2. Zener Diode Equivalent Circuits

1.1 (Cont.)
to calculate the resulting currents and terminal voltages. If the results agree with the assumed mode, the analysis is complete. For example, if the diode is assumed to be forward biased and the resulting current is in the forward direction and the terminal voltage exceeds V_d, then the assumption is valid and the solution is completed.

On the other hand, if the current and terminal voltage calculated using the particular equivalent circuit corresponding to the assumed mode of operation (Figure A-2) contradict the current direction and terminal voltage required to make the equivalent circuit valid, then the analysis is completely invalid and it will be necessary to choose one of the remaining equivalent circuits and repeat the analysis until a valid result is obtained. In actual practice, the analysis process is not quite as bleak as indicated above since the appropriate equivalent circuit is usually found on the first assumption; only rarely is a second analysis necessary. In fact, if a Zener diode is imbedded in a network, it is usually good practice to assume the diode to be an open circuit (essentially using only r_r as the equivalent circuit for the diode and assuming r_r is much larger than the network's impedance, thus considering the diode as an open circuit) and to calculate the network's input signals required to produce a diode terminal voltage of V_d or $-V_z$. If the network's input signals exceed the bounds set by the V_d and $-V_z$ breakpoints then the appropriate equivalent circuit can readily be selected and a valid solution will result.

1.2 THE BIPOLAR JUNCTION TRANSISTOR (BJT) MODEL USING ZENER DIODES

The basic bipolar junction transistor (BJT) consists of two equivalent diodes in such a close configuration that the fields of the two diodes interact. The two-diode concept as depicted in Figure A-3 is convenient for investigating the large signal behavior of a transistor. The Zener voltage for the base-emitter diode is assigned the value BV_{EBO}, the breakdown voltage emitter to base; whereas, the Zener voltage for the base-collector diode is assigned the value of BV_{CBO}, the breakdown voltage collector to base. The current-controlled current generator βi_b is active



(a) NPN Transistor

(b) PNP Transistor

Figure A-3. Large Signal Model for Bipolar Junction Transistors Using Zener Diodes

1.2 (Cont.)
only when the base-emitter diode is forward biased; the βi_b generator is zero when the base-emitter diode is reverse biased or in the Zener breakdown mode.

The various modes of transistor operation are determined by the operating state of the two diodes used in the transistor equivalent circuit. The active transistor characteristics are exhibited when the base-emitter diode is forward biased and the collector-base diode is reverse biased. In the active mode of operation the base-emitter input driving point impedance (DPI) is h_{ie} and the terminal currents are related by $i_e = i_b + i_c$, where

$$i_c = \beta i_b \text{ and } i_e = (1 + \beta)\, i_b. \tag{A-1}$$

The forward-bias breakpoint of the base-emitter diode defines the cutoff point; whereas, the forward-bias breakpoint of the collector base diode defines the saturation point. There are many modes of operation for the simple transistor because of the various combinations of conduction associated with the two equivalent diodes. Since there are two diodes with three states each, there are $3^2 = 9$ modes of operation for the single transistor. These nine modes are tabulated in Table A-1.

TABLE A-1

TRANSISTOR MODES OF OPERATION

Mode (Diode Status)			Comments
No.	BE Diode	BC Diode	
1	rev.	rev.	Cutoff Region
2	rev.	for.	Collector-Base Conduction When $V_C < V_B$ $V_E > V_B$
3	rev.	BD	Collector-Base Breakdown When $V_C > V_B$ $V_E > V_B$
4	for.	rev.	Active Region
5	for.	for.	Saturation Region
6	for.	BD	Collector-Emitter Breakdown {or Base-emitter for biased & V_C high enough for BD.
7	BD	rev.	Base-Emitter Breakdown
8	BD	for.	Emitter-Collector Breakdown or $V_B < V_E$ & $V_B > V_C$
9	BD	BD	Usually Impossible Unless R_E &/or R_C external resistors are present.

It is not necessary to memorize Table A-1 in order to investigate transistor circuits for upset and damage resulting from an EMP condition; it is usually sufficient to realize that the transistor does, under large signal excitation, exhibit the two-Zener diode equivalent circuit behavior and that conduction paths are possible between any pair of terminals regardless of the polarity of the EMP excitation. By using a systematic approach, all worse-case damage and upset conditions can be found.

1.3 CIRCUIT EXAMPLE

The circuit shown in Figure A-4 is chosen as a test circuit to illustrate the various modes of transistor operation that can be experienced when transient input signals are impressed on the base, emitter, collector, and power supply terminals. The basic circuit consists of a single NPN transistor whose base is biased by the voltage divider consisting of R_1 and R_2, and whose collector and emitter loads are R_C and R_E, respectively. The

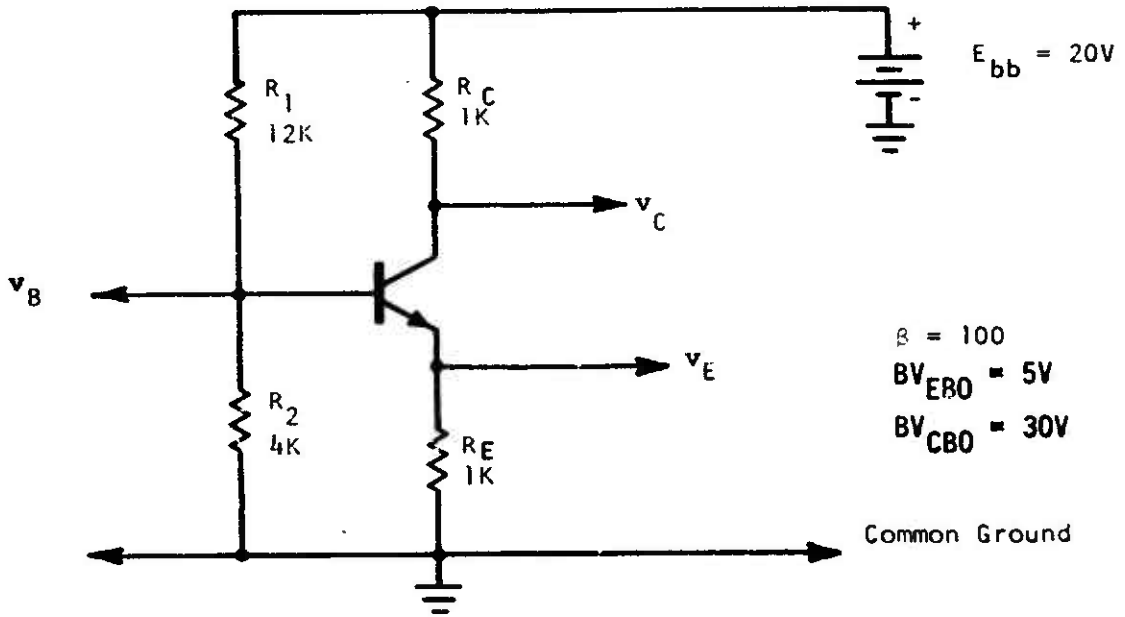


Figure A-4. Example Test Circuit to Illustrate Transistor Modes of Operation

1.3 (Cont.)

R_1-R_2 voltage divider establishes a base voltage of approximately 5 volts and the emitter potential follows the base voltage by emitter follower action (actually the emitter voltage is one diode drop lower in potential than the base, but this baae-emitter drop will be neglected here for simplicity). Thus, both V_{BQ} and E_{EQ} are approximately +5 volts. The quiescent emitter current is approximately 5 ma = (V_{EQ}/R_E), and with a high-β transistor, the collector current is also about 5 ma. The collector voltage is found as $E_{bb} - I_C R_C \approx +15$ volts. Therefore, the transistor is operating in its active mode with its B-E diode forward biased and its collector-base diode reverse biased (mode 4; Table A-1).

1.4 BASE INPUT TRANSIENT

The test circuit is first subjected to an input signal applied to its base terminal as shown in Figure A-5. When E_{iB} rises positively from zero, the transistor is taken through its active region (Figure A-6). At $E_{iB} \approx +10_v$. The collector potential has dropped to base and emitter potential and the saturation point is reached. Further increase in E_{iB} carries the transistor farther into the saturation region (mode 5, Table A-1). In the saturation mode, the collector, base, and emitter potentials are approximately equal.

As the base input signal takes negative excursions, the transistor first experiences the cutoff region (mode 1; Table A-1), then the base-emitter breakdown region (mode 7, Table A-1), and finally collector-base breakdown occurs in addition to base-emitter breakdown (mode 9, Table A-1). Thus, transient input signals impressed on the baae of a transistor, which has both a collector resistor R_C and an emitter resistor R_E, will cause the transistor to experience five (5) possible modes of operation. The worse case with reapect to possible transistor damage occurs in mode 9 where both the base-emitter and the base-collector junctions are operating in the reverse breakdown mode.

Referring to Figure A-6(a), it should be noted that the plot of v_B, v_C, and v_E versus E_{iB} are designated as the transfer characteristic curves since the

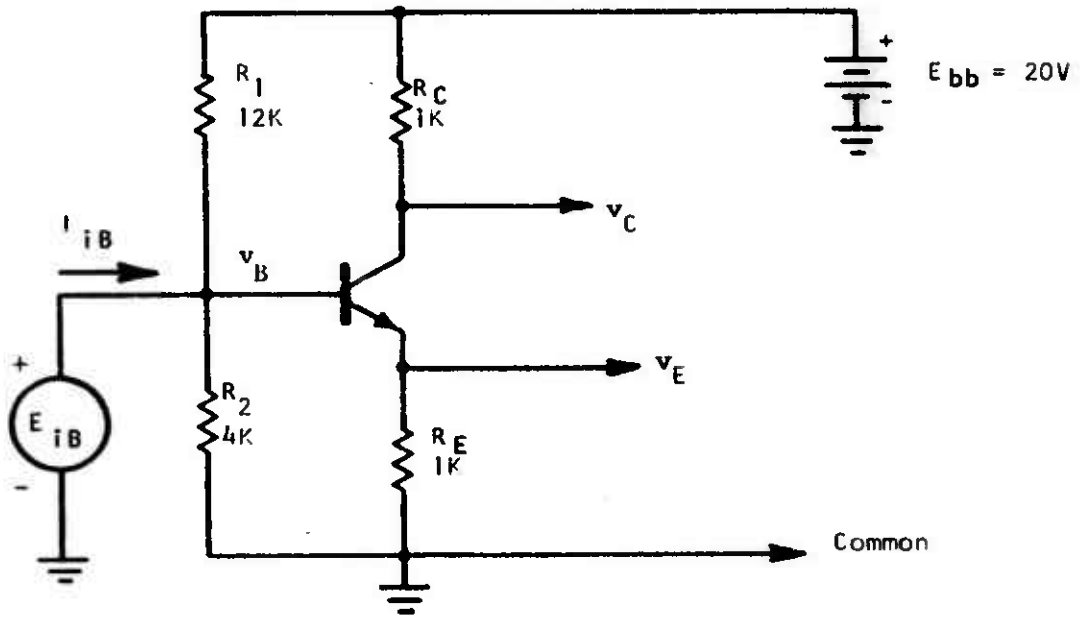


Figure A-5. Transistor Test Circuit with Input Applied Directly to the Base Terminal

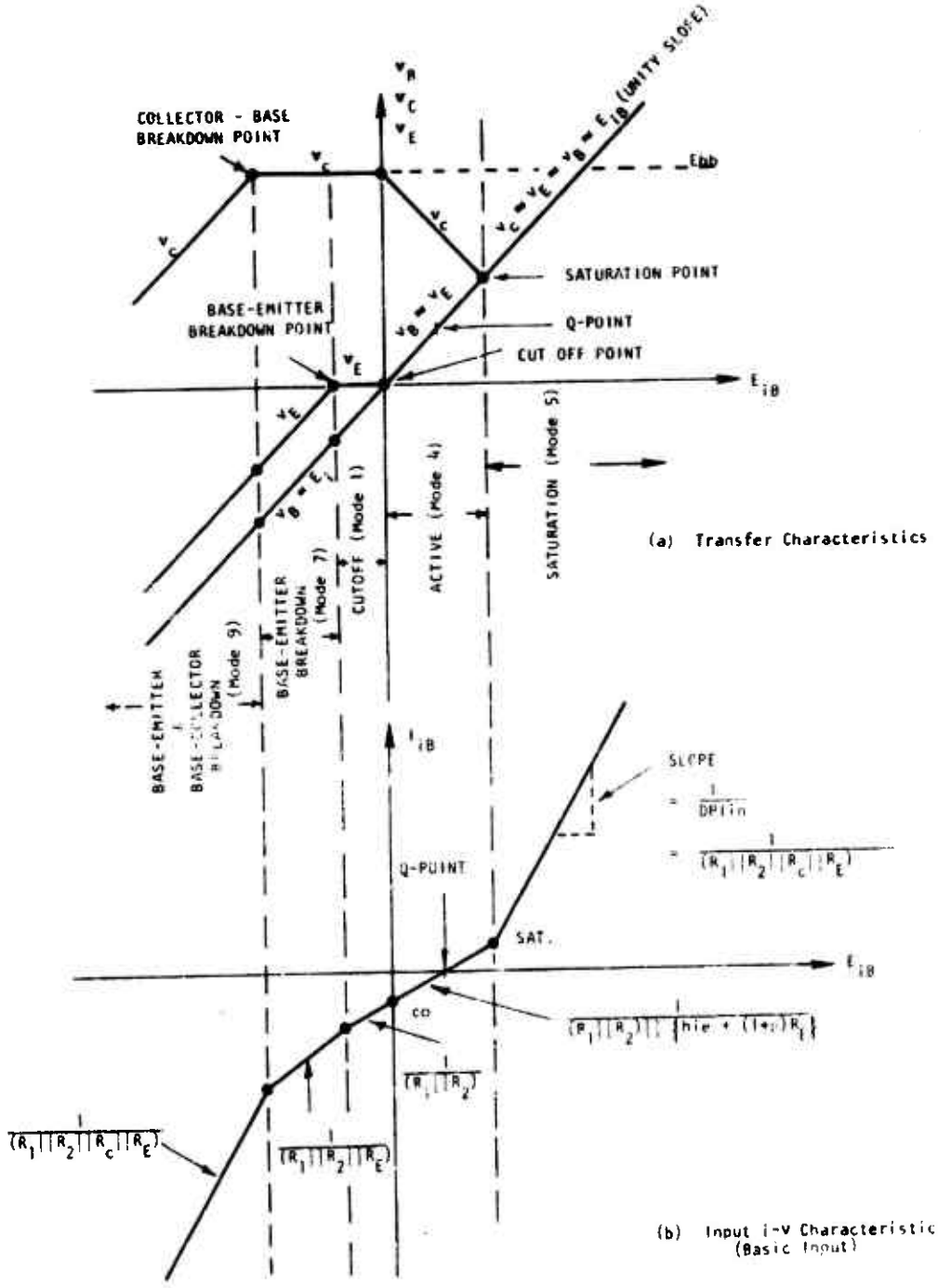


Figure A-6. Base Input Characteristics of Transistor Test Circuit

1.4 (Cont.)

respective slopes denote the circuit gain from the E_{iB} input to the output represented by a given curve. It should be also pointed out that the plot of v_B versus E_{iB} is the unity-slope line since E_{iB} is applied directly to the base and the v_B curve thus represents E_{iB} versus E_{iB}. A similar relationship will apply to any electrode upon which the input signal is impressed.

In Figure A-6(b) is shown the current-voltage characteristic of the transistor test circuit as seen by the E_{iB} signal source. Of particular note is the fact that the slope of the i-v curve represents the driving-point admittance (the reciprocal of the slope represents input driving-point impedance, DPI_{in}) as seen by the E_{iB} signal source. It is noted that DPI_{in} is different for each mode of operation. The DPI_{in} values are found as the series-parallel combination of impedances exhibited by the simplified equivalent circuit that applies to the given mode of operation. A shorthand notation is used to denote the DPI_{in} experienced in each mode where $(R_1||R_2)$ denotes the parallel combination of resistors R_1 and R_2, etc. (see Appendix C).

1.5 EMITTER INPUT TRANSIENT

Shown in Figure A-7 is the same transistor test circuit, but with the input transient signal impressed upon the emitter. The different modes of transistor operation experienced for an emitter-input excitation are shown in Figures A-8(a) and A-8(b). Notice that only a narrow active range exists, but that four other modes of operation are also permissible; namely, saturation, cut-off, base-emitter breakdown, and emitter-collector breakdown (mode 8; Table A-1). The worse case with regard to possible transistor damage occurs in mode 8, emitter base breakdown, which takes place for large positive (+) input signals. Five modes of transistor operation exist.

1.6 COLLECTOR INPUT TRANSIENT

In Figure A-9 is shown the same transistor test circuit being driven by an input signal applied to the collector terminal. The resulting modes to which the transistor is subjected by this collector input signal are depicted in

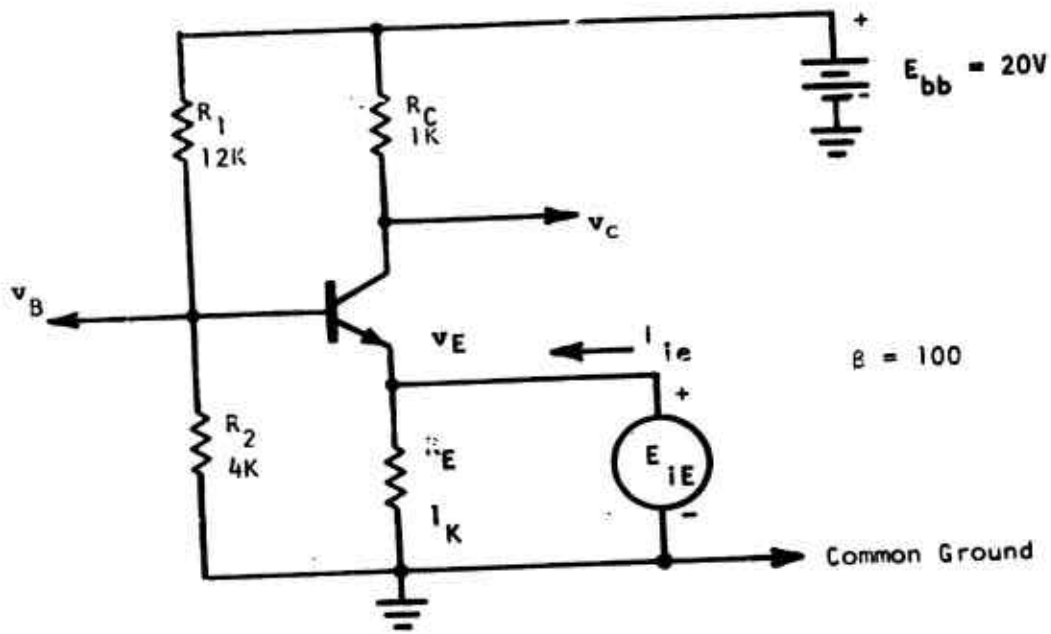


Figure A-7. Transistor Test Circuit with Input Signal Applied to Emitter Terminal

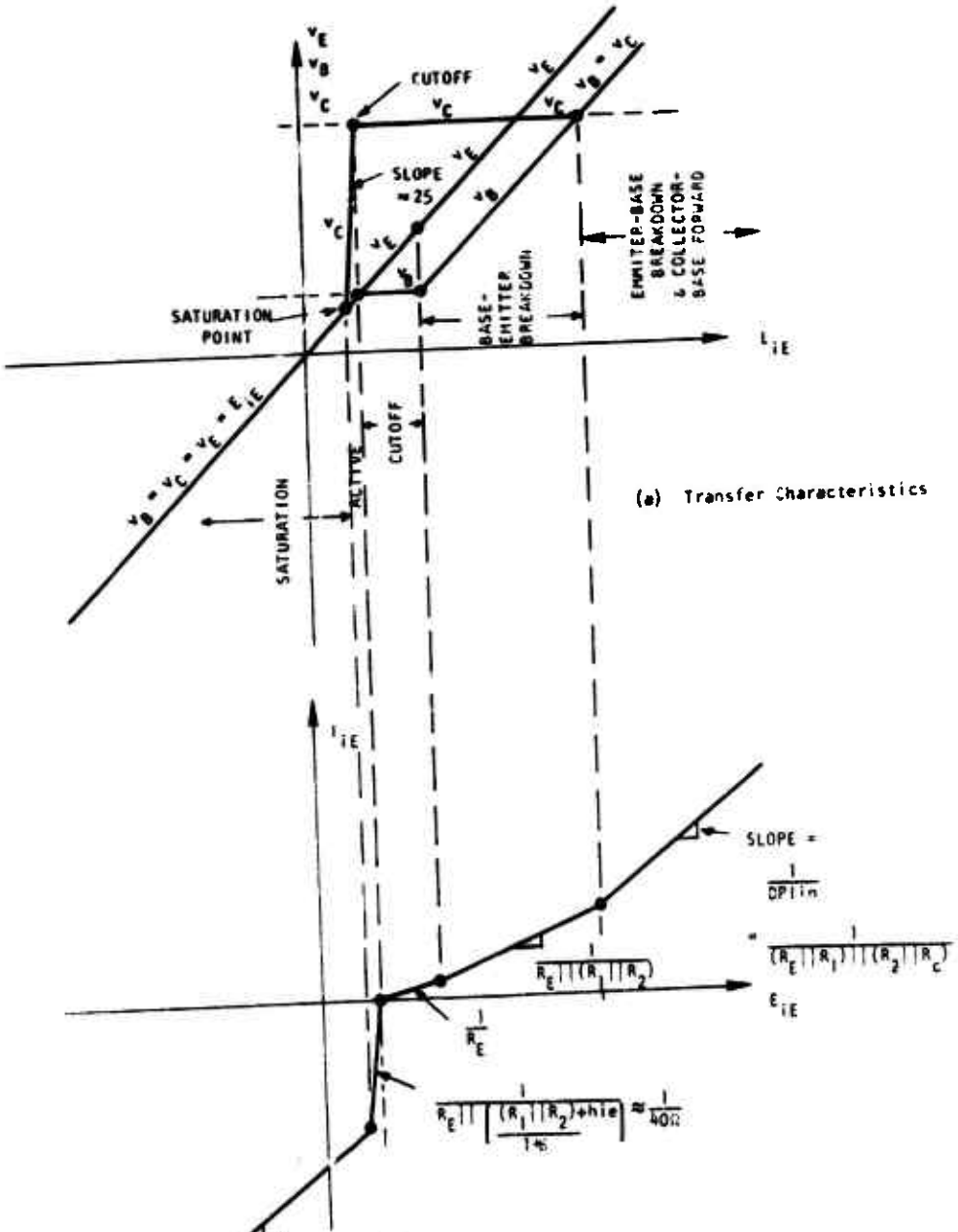


Figure A-8. Emitter Input Charscteristics of Trsnsistor Test Circuit

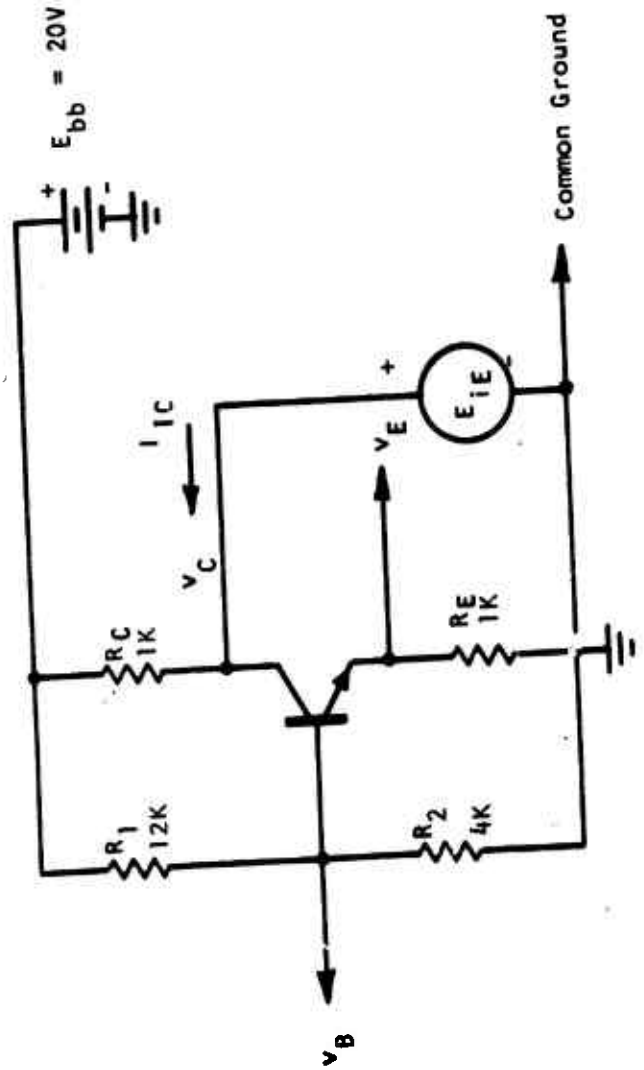


Figure A-9. Transistor Test Circuit with Input Signal Applied to the Collector Terminal

1.6 (Cont.)

Figure A-10(a) and A-10(b). The active region is quite large, but eventually collector-base breakdown occurs for a sufficiently high positive (+) input signal. The worse case condition for possible transistor damage occurs for a high positive input signal which causes collector-base breakdown. Five possible modes of operation are experienced.

1.7 POWER SUPPLY BUSS INPUT TRANSIENT

When the input transient is impressed upon the E_{bb} buss as shown in Figure A-11, an interesting case exists. In order to find the driving point impedance existing in the active region (Figure A-12), a derivation of the feedback amplifier configuration is performed. Because this DPI_{in} value is difficult to evaluate, a short derivation is presented as an additional note. There are two worse case modes to consider; for high positive input values, collector-emitter breakdown takes place; whereas, for large negative inputs there is breakdown from emitter to collector.

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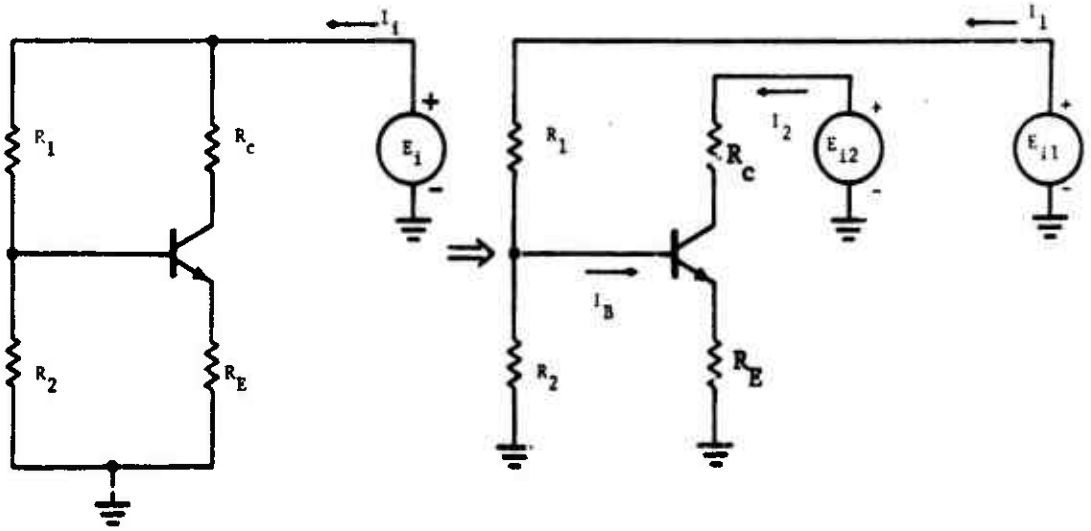
* Note: Derivation of DPI seen by E_{bb} in active region; Figure A-12.



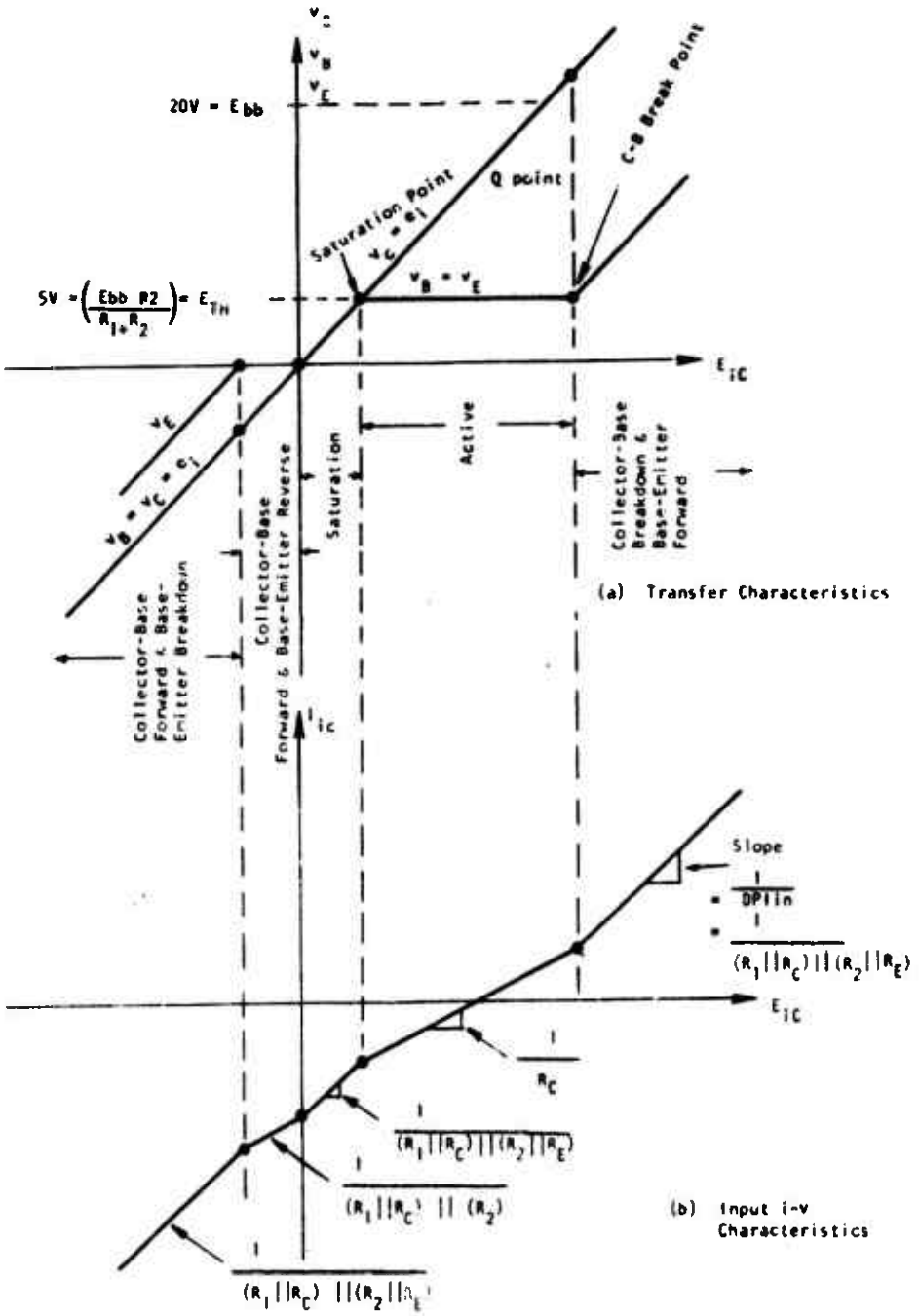


Figure A-10. Collector Input Charscteristics of Transistor Test Circuit

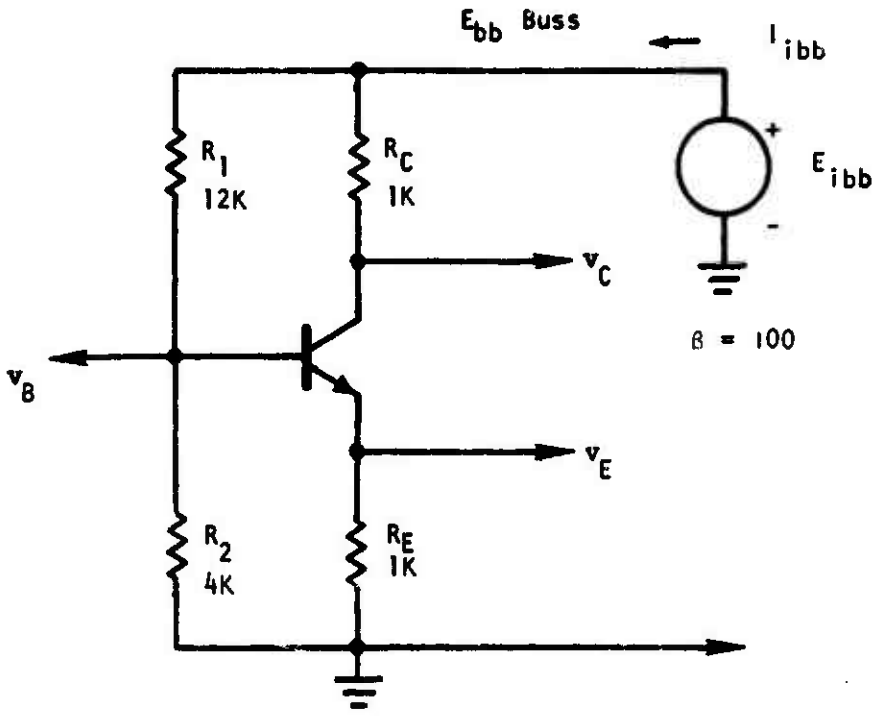


Figure A-11. Transistor Test Circuit With Input Signal Applied to Power Supply Buss

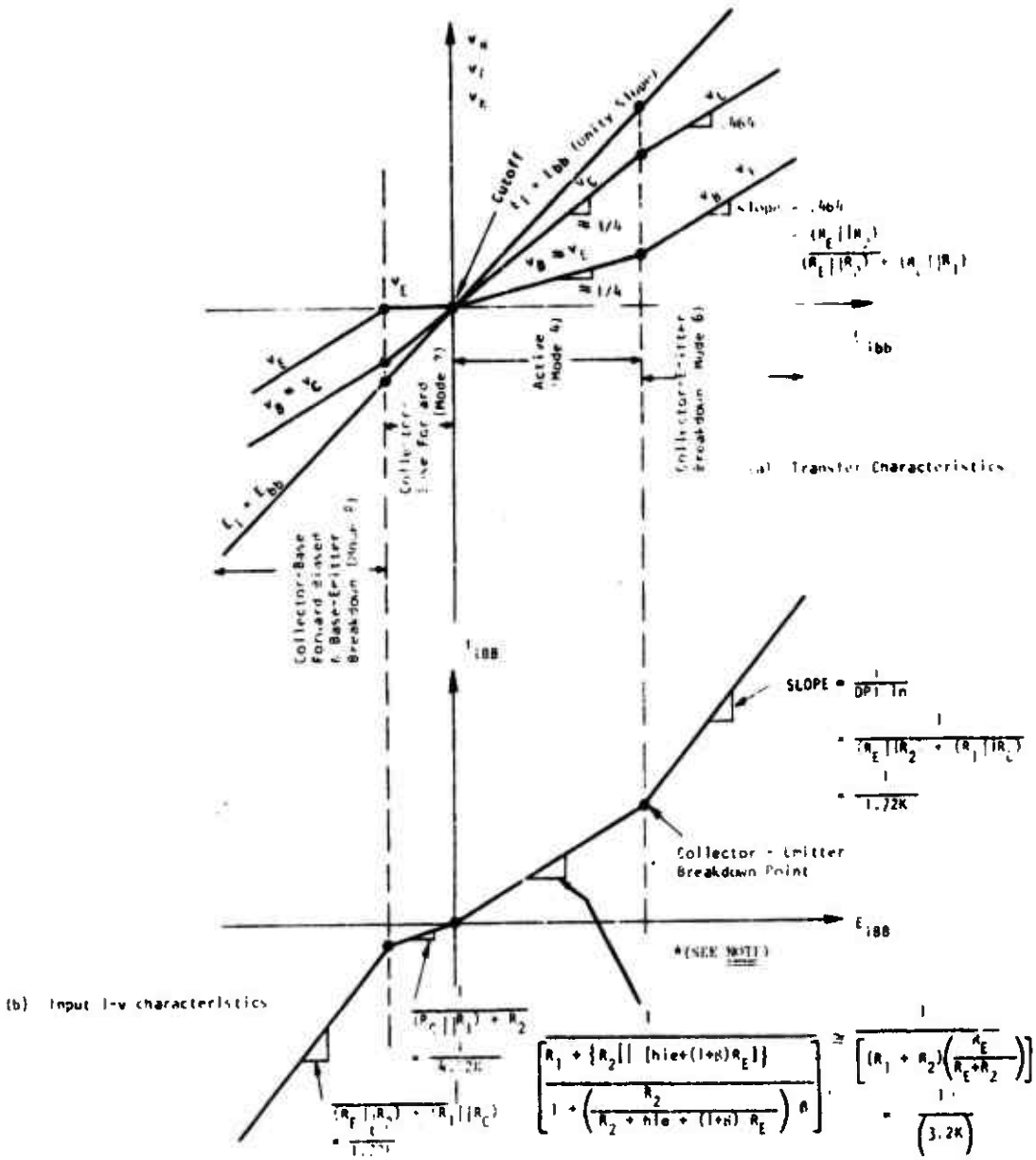


Figure A-12. Power Supply Input Characteristics of Transistor Test Circuit

1.7 (Cont.)
Note (Cont.)

$$DPI_{in} = \frac{E_i}{I_i}$$

$$I_1 = I_{11} + I_{12}$$

$$I_2 = I_{22} + I_{21}$$

where I_{12} = current in No. 1 circuit caused by E_{i2}

I_{21} = current in No. 2 circuit caused by E_{i1}

By superposition (and DPI):

$$I_{11} = \frac{E_{i1}}{R_1 + \left[R_2 \,||\, \left\{h_{ie} + (1 + \beta)\, R_E\right\}\right]}$$

$$I_{21} = I_B\, \beta = I_{11} \left[\frac{R_2}{R_2 + \left\{h_{ie} + (1 + \beta)\, R_E\right\}}\right] \beta$$

I_{22} = Zero and I_{12} = Zero

$\therefore$ Setting $E_{i1} = E_{i2} = E_i$ the total $I_i = I_{11} + I_{21}$

$$I_i = \left[\frac{E_i}{R_1 + \left[R_2 \,||\, \left\{h_{ie} + (1 + \beta)\, R_E\right\}\right]}\right] \left\{1 + \left[\frac{R_2}{R_2 + \left\{h_{ie} + (1 + \beta)\, R_E\right\}}\right] \beta\right\}$$

$$I_i = \frac{E_i}{DPI_{in}} = \left\{ \frac{\dfrac{E_i}{R_1 + \left[R_2 \,||\, \left\{h_{ie} + (1 + \beta)\, R_E\right\}\right]}}{1 + \left[\dfrac{R_2}{R_2 + \left\{h_{ie} + (1 + \beta)\, R_E\right\}}\right] \beta} \right\}$$

1.7 (Cont.)

Note (Cont.)

$$\text{Therefore } DPI_{in} = \left[\frac{R_1 + \left[R_2 \,||\, \left\{ h_{ie} + (1 + \beta)\, R_E \right\} \right]}{1 + \left[\frac{R_2}{R_2 + \left\{ h_{ie} + (1 + \beta)\, R_E \right\}} \right]^{\beta}} \right]$$

for high-β transistor where

$$\left[h_{ie} + (1 + \beta)\, R_E \right] >> R_2 \quad \text{and} \quad \left[(1 + \beta)\, R_E \right] >> h_{ie}$$

$$DPI_{in} \approx \left[R_1 + R_2 \right] \left[\frac{R_E}{R_E + R_2} \right]$$

$$= (12\ K + 4\ K) \left[\frac{1\ K}{5\ K} \right] = \frac{16\ K}{5} = \boxed{3.2\ K}$$

1.8 VARIATIONS OF THE BASIC TEST CIRCUIT

The basic test circuit described above was presented to demonstrate the modes of transistor operation which one could experience under various input signal conditions. It would be almost an endless task to consider all variations of the basic test circuit, but the above discussion should alert the circuit designer to the various aspects of transistor operation that can be expected when one deviates from the normal operating region. If certain resistance values; namely, R_C or R_E, have zero value, then the entire circuit results presented above would be altered and some very severe damage conditions could exist. In the above test circuit, the large external resistor values protected the transistor from damage unless extremely large transient signals were experienced. In fact, bulk resistance was completely ignored because in comparison to the external resistors, bulk resistance would be swamped out. However, if either R_E or R_C were zero (or bypassed with large capacitors), then input currents in these cases would be limited only by bulk resistance or the signal source impedance.

1.8 (Cont.)

When analyzing a circuit such as a saturated switching circuit for upset, one may have to consider all nine modes of transistor operation listed in Table A-1. Although the circuit operates normally between the cutoff and saturation regions (modes 1 and 5) the transient upset signal can drive the transistors of interest into any of the listed modes. For some upset analyses, the n-parameter small signal model of a transistor may be used. For this model parameters such as β, h_{ie}, h_{oe}, etc. are used. This model is discussed in most references on transistors, and therefore will not be discussed further.

1.9 COMPUTER AIDED ANALYSIS MODELS

Currently, most transient analysis computer programs utilize modified Ebers-Moll models of the diode and transistor or their charge-control equivalent. In their normal form such models do not predict breakdown and are probably not valid for high forward junction currents. A typical modified Ebers-Moll model is shown in Figure A-13 for an NPN transistor. The capacitors C_C and C_E and resistors R_{bb} and R_{cc} are modifications made to account for turn-on time, turn-off time, storage time and bulk resistance. The current I_{rc} is generally represented by an equation of the form $I_{rc} = I_{ES}\ (e^{\theta v_{rc}} - 1)$ where v is the voltage across the junction and I_{ES} is the junction reverse short circuit current (positive voltage responds to forward bias voltage). For large negative voltage $I_{rc} = I_{ES}$. Thus, the transistor model can be seen to predict a reverse current I_{ES} for all negative voltages. In reality, once the reverse avalanche voltage of the junction is exceeded (breakdown occurs) a large negative current will flow. This breakdown phenomena will have to be added if computer codes are used for damage analysis and for some upset analyses. Consider also the base resistance R_{bb}. In the computer upset analysis example predicted in the EMP Susceptibility Threshold Analysis Handbook R_{bb} was obtained for a 2N705 transistor operating at base low currents. Its value was determined to be 50Ω. Even in the upset analysis the normal base currents of the "on" transistor are approximately 6 ma. This results in a voltage drop across R_{bb} of 0.3V which, when added to an approximate germanium junction voltage of 0.3V, yields a rather high base-emitter terminal voltage of 0.6V. At the high currents required for forward junction damage this resistance would result in erroneously high terminal voltages and powers.

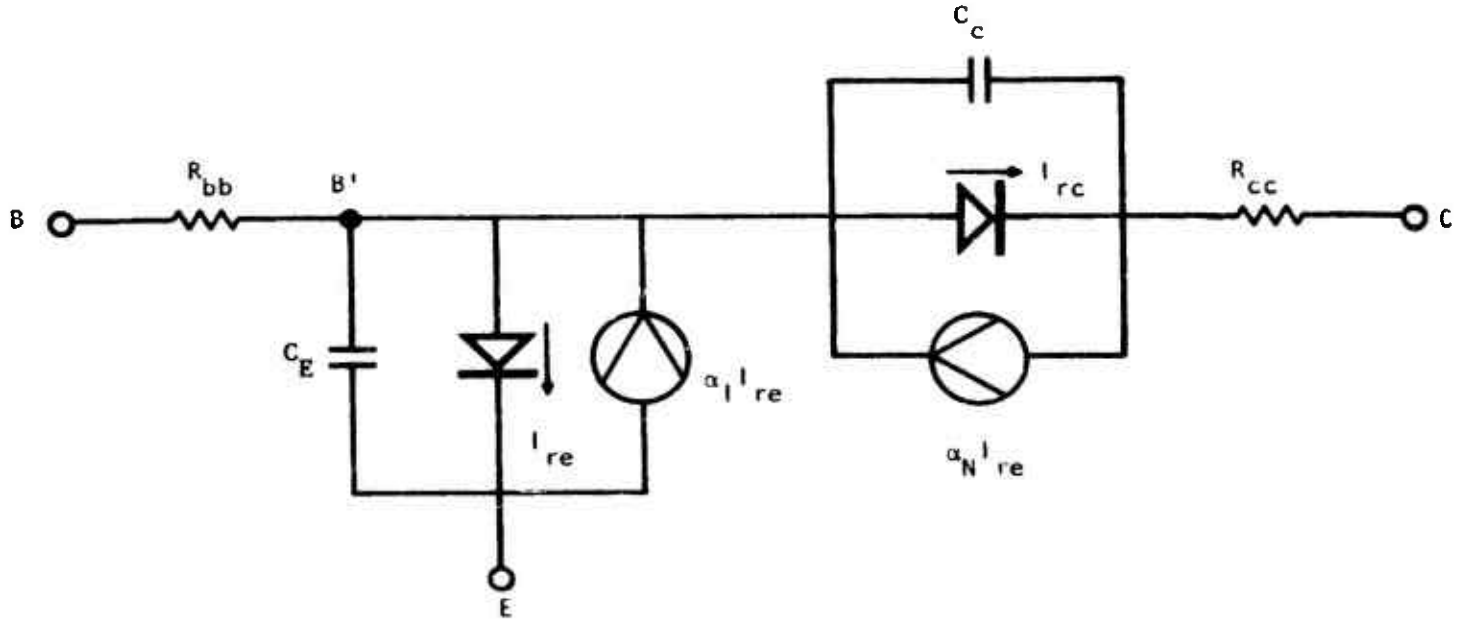


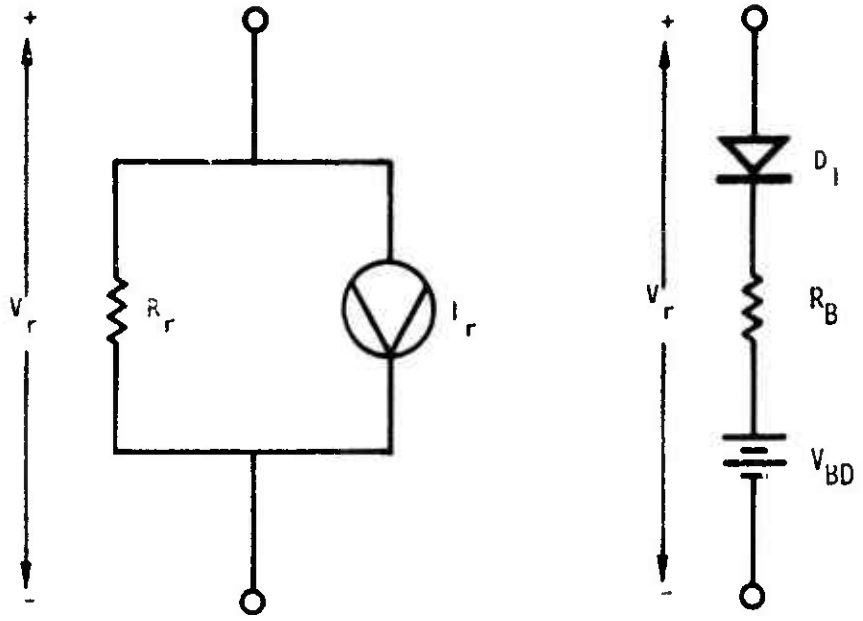
Figure A-13. Modified Ebers-Moll Transistor Model

1.9 (Cont.)

Computer models for junction semiconductors may be modified to account for breakdown by placing the model used in hand analysis for reverse breakdown across each junction, provided the analyst has an electrical model of the Zener diode available. Other elements which can be used to shunt these junctions are shown in Figure A-14. In the (a) portion of this figure the resistance R_r is made large so as not to interfere with normal junction parameters. I_r is then made a mathematical function of the voltage across R_r to yield the desired V-I reverse characteristic. In the (b) portion of Figure A-14 the diode D1 is an ideal diode and is used to prevent current flow due to V_{BD} until the breakdown voltage is exceeded. V_{BD} is given the value of the junction breakdown voltage and R_B the value of the reverse direction bulk resistance. The models are placed in the circuit such that the polarities indicated for V_r will reverse bias the shunted junction.

Breakdown and high current injection effects may be incorporated in the basic transistor model more elegantly by modifying the mathematical relations for junction voltage and current and making R_{bb} and/or R_{cc} a current dependent resistor (Reference 16). However, within the present limits of upset and damage analysis accuracy the above mentioned shunting models are felt to be adequate for any contemplated computer damage analyses.

In most computer analyses programs one can define his own models. For example, a low frequency h-parameter model of a transistor such as shown in Figure A-15 could be used in a dc threshold upset analysis. This model could be made more sophisticated by the addition of input and output capacitances. The information needed to construct this model is usually available from manufacturer's data sheets.



(a) Current Model

(b) Voltage Model

Figure A-14. Computer Breakdown Models

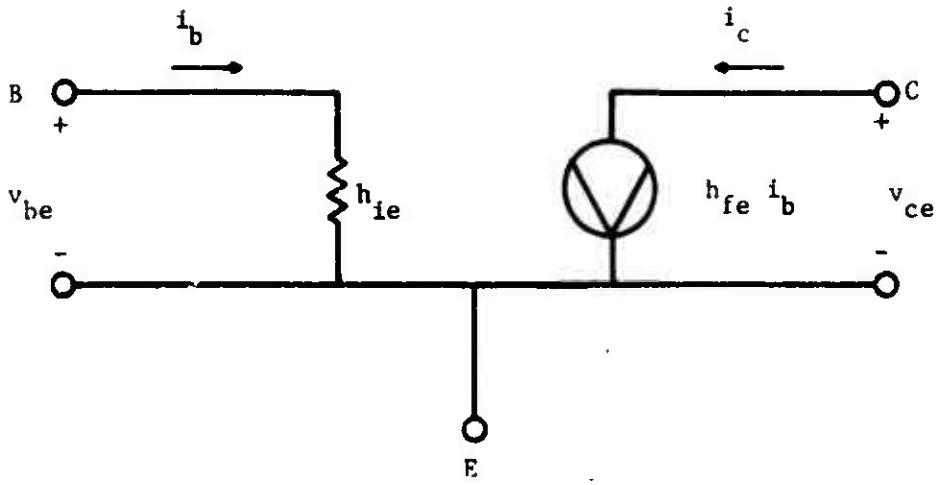


Figure A-15. Simplified n-parameter Model of a Transistor

APPENDIX B
DAMPED SINE WAVE TO RECTANGULAR PULSE CONVERSION FOR EQUIVALENT PERMANENT DAMAGE

The damage constant, K, derived by Wunsch (Reference 11) for semiconductor junction devices is based on a rectangular pulse. However, the B-1 bulk cable current specification is given in terms of a damped sine wave. To be able to use the Wunsch damage constant one must be able to relate the period of the damped sine wave τ_s to the period of a rectangular pulse τ_p, of the same peak amplitude, that produces the same device damage. For a sinusoidal waveform, junction failure may occur in either the forward or the reverse bias direction. Failure in the forward bias direction is most likely to occur when the source impedance is small and cannot effectively limit junction current to non-destructive levels. In this case the voltage of the generator need not exceed the breakdown voltage of the device. Reverse bias failure will occur when the source impedance is sufficient to limit the forward current to a non-destructive level but will permit failure level reverse current to flow. In many cases the current required to produce failure in the forward direction is much larger than the current ·se required in the reverse direction.

The Wunsch expression for the power required to cause junction failure for a rectangular pulse is

$$P_F = Kt_F^{-1/2} \qquad \text{(B-1)}$$

where K is a device dependent constant and t_F is the time to failure. The energy required to fail the device is

$$E_F = \int_0^{t_F} Kt_F^{-1/2}\, dt \qquad \text{(B-2)}$$

or

$$E_F = Kt_F^{1/2} \tag{B-3}$$

where E_F is the failure energy. Equation (B-3) may also be written as

$$K = E_F t_F^{-1/2} \tag{B-4}$$

Since K is device dependent and is independent of waveform one can use this expression to equate the failure energies and times of various waveforms. That is

$$E_{F1} t_{F1}^{-1/2} = E_{F2} t_{F2}^{-1/2} . \tag{B-5}$$

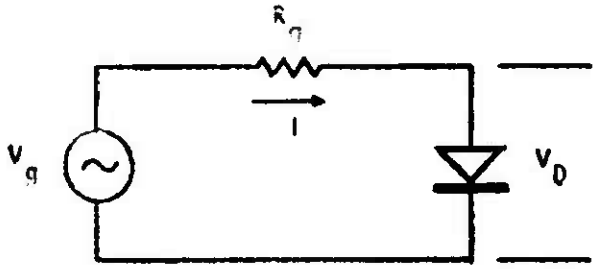
Consider the simple circuit shown in Figure B-1a. For a positive going rectangular pulse at the generator of amplitude V_o ($V_o \gg V_D$), the current through the device is

$$I_o \approx \frac{V_o}{R_g} . \tag{B-6}$$

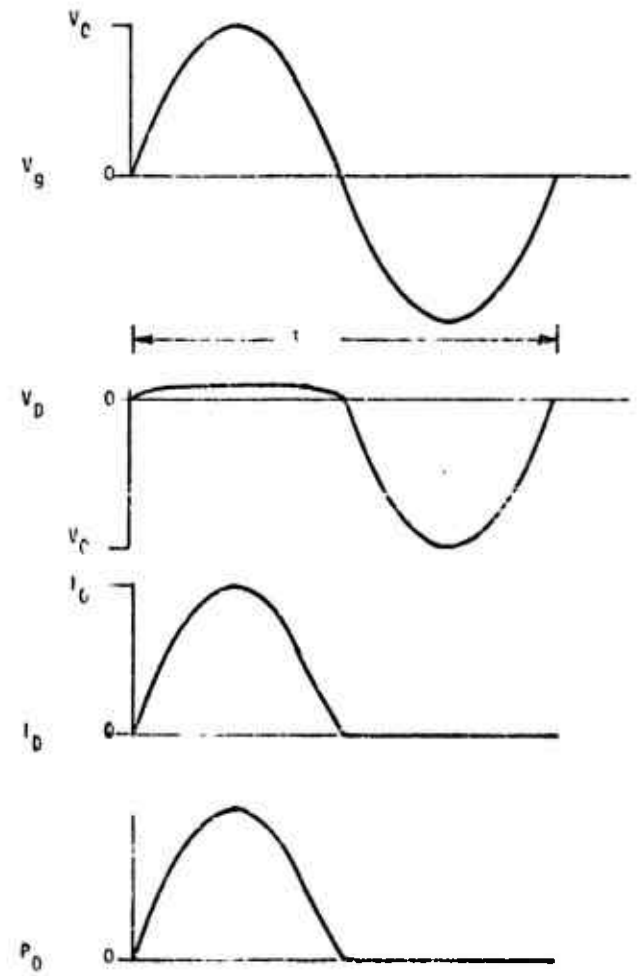
The energy absorbed by the device during the pulse is

$$E_p = V_D I_o \tau_p \tag{B-7}$$

where τ_p is the pulse width. If this pulse is just sufficient to fail the device then



(a) Simple Circuit Analyzed for $V_g < V_{BD}$



(b) Device Waveforms for $V_g < V_{BD}$

Figure B-1. $V_g < V_{BD}$

$$\tau_p = \tau_F \tag{B-8}$$

and

$$E_p = E_F \tag{B-9}$$

Substituting these quantities into Equation (B-4), the damage constant for the device is

$$K_p = V_D I_o \tau_p^{1/2} \tag{B-10}$$

where the p aubscript indicates that the damage constant was obtained for a rectangular pulse.

For the same circuit (Figure B-1), assume a sine wave generator voltage. If the input signal does not exceed the breakdown voltage, the waveforms of Figure B-1b will hold.

It is assumed that the device loading will not cause distortion of the generator waveform. The input voltage, V_g, is

$$V_g = V_o \sin \omega t \tag{B-11}$$

where ω is the radian frequency, but

$$\omega = 2\pi f = \frac{2\pi}{\tau_s} \tag{B-12}$$

so that

$$V_g = V_o \sin \frac{2\pi t}{\tau_s} \tag{B-13}$$

where τ_s is the period of the sine wave. The current during the conducting portion of the cycle is written as

$$I = I_o \sin \frac{2\pi t}{\tau_s} \qquad 0 \leq t \leq \frac{\tau_s}{2} \tag{B-14}$$

where

$$I_o \approx \frac{V_o}{R_g} \tag{B-15}$$

and

$$V_D = \text{Constant} \qquad 0 \leq t \leq \frac{\tau_s}{2} \tag{B-16}$$

The energy absorbed by the device during conduction is

$$E_s = \int_o^{\frac{\tau_s}{2}} V_D I \, dt \tag{B-17}$$

or

$$E_s = \int_o^{\frac{\tau_s}{2}} V_D I_o \sin \frac{2\pi t}{\tau_s} \, dt \tag{B-18}$$

Performing the integration, one obtains

$$E_s = \frac{V_D I_o \tau_s}{\pi} \tag{B-19}$$

If the sine wave is just sufficient to cause failure in the forward bias direction, then

$$\frac{\tau_s}{2} = t_F \tag{B-20}$$

and

$$E_s = E_F \tag{B-21}$$

using these quantities in Equation (B-4), the damage constant is

$$K_s = \frac{\sqrt{2}\ V_D\ I_o}{\pi}\ \tau_s^{1/2} \tag{B-22}$$

where the s subscript indicates that K was obtained from a sine wave.

K_p and K_s (Equations B-10 and B-22) are equated giving

$$V_D I_o \tau_p^{1/2} = \frac{\sqrt{2}\ V_D I_o}{\pi}\ \tau_s^{1/2} \tag{B-23}$$

or

$$\tau_p = 0.203\ \tau_s \tag{B-24}$$

but

$$\tau_s = \frac{1}{fs} \tag{B-25}$$

therefore

$$\tau_p \approx \frac{1}{5f_s} \qquad \text{(B-26)}$$

Equations (B-24) snd (B-26) show the relation between s sine wave of a given frequency or period and the pulse width of a square pulse necessary to produce the same forward bias damage.

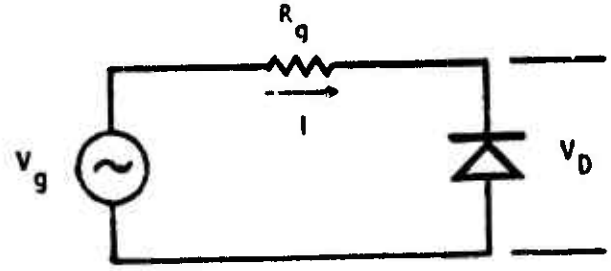
In the case where the input voltage exceeds the junction breskdown voltage and failure is assumed to occur in the reverse bias direction, the circuit shown in Figure 2s will be used for the analysis The analysis based on a rectangular pulse for reverse breakdown is the same as for the forward case except that the expression for I_o is now

$$I_o = \frac{V_o - V_{BD}}{R_g} \qquad \text{(B-27)}$$

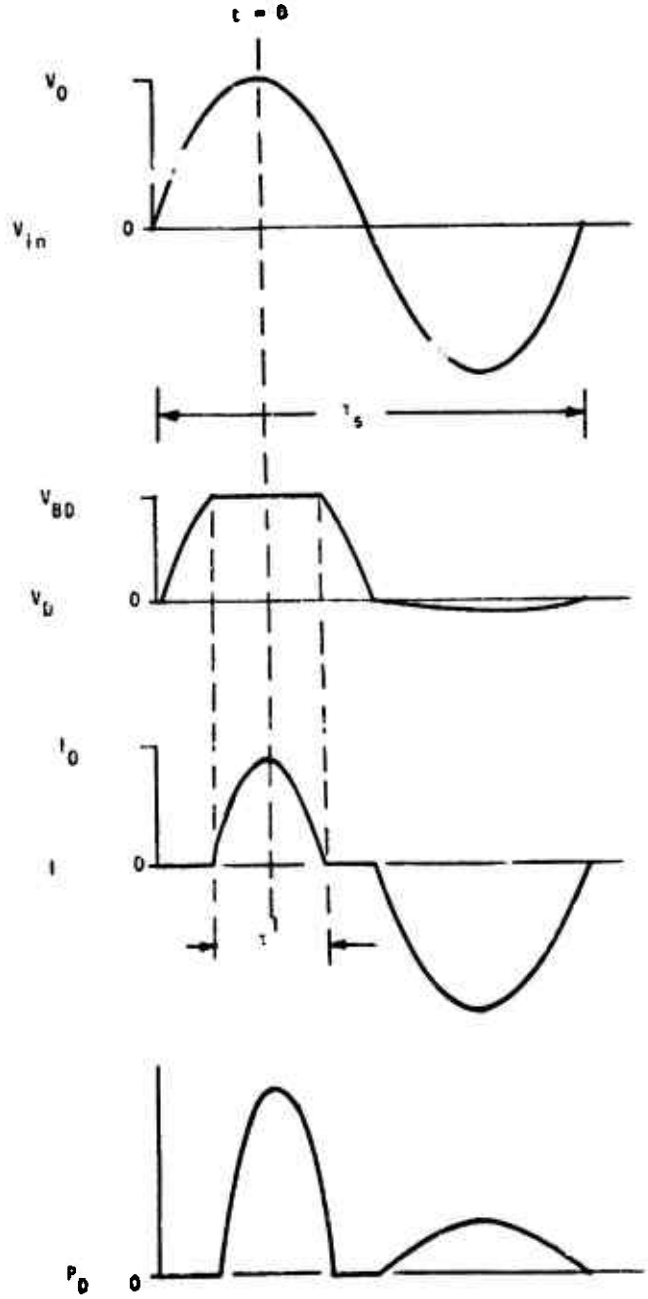
where V_{BD} is the reverse breskdown voltage of the device. The damage constant K_p in this csse is still given by Equation (B-10) with I_o given by Equation (B-27). As ststed by Wunsch, K_p does not have the same numerical value for the forward bias and reverse biss csses, only the same general expression.

For a sine wave applied to the circuit of Figure B-2s, the waveforms shown in Figure B-4 will hold. These waveforms are not drawn to scale and are used only to indicate relative wsveshapes. To simplify the snalysis, the t = 0 point has been shifted as shown in Figure B-2b. The input voltage is, therefore

$$V_g = V_o \cos \frac{2\pi t}{\tau_s} \qquad \text{(B-28)}$$



(a) Simple Citcuit Analyzed for $V_g > V_{BD}$



(b) Device Waveforms for $V_g > V_{BD}$

Figure B-2. $V_g > V_{BD}$

During the time that the input voltage exceeds the device breakdown voltage

$$V_D = V_{BD} \quad , \quad -\frac{\tau'}{2} \leq t \leq \frac{\tau'}{2} \tag{B-29}$$

and

$$I = I_o \cos \frac{2\pi t}{\tau_s} \quad , \quad -\frac{\tau'}{2} \leq t \leq \frac{\tau'}{2} \tag{B-30}$$

where

$$I_o = \frac{V_o - V_{BD}}{R_g} \tag{B-31}$$

The energy absorbed by the device during breakdown is

$$E_s = \int_{-\frac{\tau'}{2}}^{\frac{\tau'}{2}} V_{BD} I_o \cos \frac{2\pi t}{\tau_s} \, dt \tag{B-32}$$

Performing the integrstion and evalusting the limits

$$E_s = \frac{V_{BD} I_o \tau_s}{\pi} \sin \frac{\pi \tau'}{\tau} \tag{B-33}$$

In order to evaluate this expression further, s relationship between τ' and τ_s is needed. Figure B-3 shows the first half cycle of the input waveform with the device breakdown and time, τ', indicsted. From this figure one can see thst when $V_g = V_{BD}$

$$t = \frac{\tau'}{2} \tag{B-34}$$

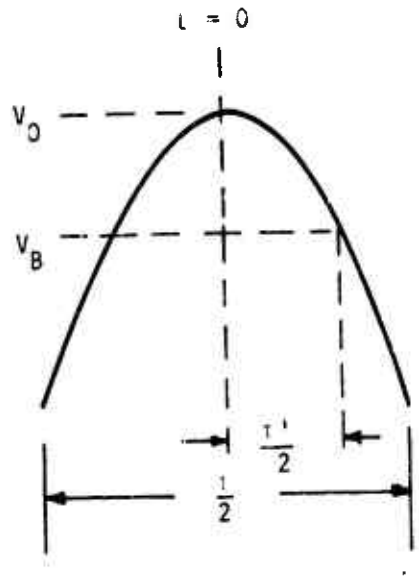


Figure B-3. Half Cycle of Sine Wave Showing the Relation Between τ and τ'.

Inserting these values in Equation (B-28), one obtains

$$\frac{V_{BD}}{V_o} = \cos \frac{\pi\tau'}{\tau_s} \qquad \text{(B-35)}$$

or

$$\tau' = \frac{\tau_s}{\pi} \text{Cos}^{-1} \frac{V_B}{V_o} \qquad \text{(B-36)}$$

Equation(B-36) is now used in Equation (B-33) to obtain

$$E_s = \frac{V_{BD} I_o \tau_s}{\pi} \sin\left[\text{Cos}^{-1} \frac{V_{BD}}{V_o} \right] \qquad \text{(B-37)}$$

but

$$\text{Cos}^{-1} \frac{V_{BD}}{V_o} = \text{Sin}^{-1} \left[1 - \left(\frac{V_{BD}}{V_o} \right)^2 \right]^{1/2} \qquad \text{(B-38)}$$

so that

$$E_s = \frac{V_{BD} I_o \tau_s}{\pi} \left[1 - \left(\frac{V_{BD}}{V_o} \right)^2 \right]^{1/2} \qquad \text{(B-39)}$$

If the time required to fail the device is the time above breakdown, then

$$\tau' = t_F \tag{B-40}$$

and

$$E_s = E_f \tag{B-41}$$

The damage constant, K, is determined by inserting Equations (B-40) and (B-41) into Equation (B-4)

$$K_s = V_{BD} I_o \left[\frac{1 - \left(\frac{V_{BD}}{V_o}\right)^2}{\pi \cos^{-1}\left(\frac{V_{BD}}{V_o}\right)} \right]^{1/2} \tau_s^{1/2} \tag{B-42}$$

Equating the damage constants K_s and K_p one obtains

$$V_{BD} I_o \tau_p^{1/2} = V_{BD} I_o \left[\frac{1 - \left(\frac{V_{BD}}{V_o}\right)^2}{\pi \cos^{-1}\left(\frac{V_{BD}}{V_o}\right)} \right]^{1/2} \tau^{1/2} \tag{B-43}$$

or

$$\tau_p = \frac{1 - \left(\frac{V_{BD}}{V_o}\right)^2}{\pi \cos^{-1}\left(\frac{V_B}{V_o}\right)} \tau_s \qquad \text{(B-44)}$$

Equation (B-44) gives the relation between the period of a sine wave and the width of a square pulse which will produce equal degradation in the reverse bias case.

Figure B-4 shows a plot of $\tau_p/$ · ersus V_o/V_{BD}. From this plot it can be seen that for values of V_o/V_{BD} greater than 1.5 the value of τ_p/τ_s approaches that predicted for the forward bias case of Equation (B-24). For values of V_o/V_{BD} less than 1.5, the ratio τ_p/τ_s differs from the forward bias case and can be read from the expanded curve of Figure B-5.

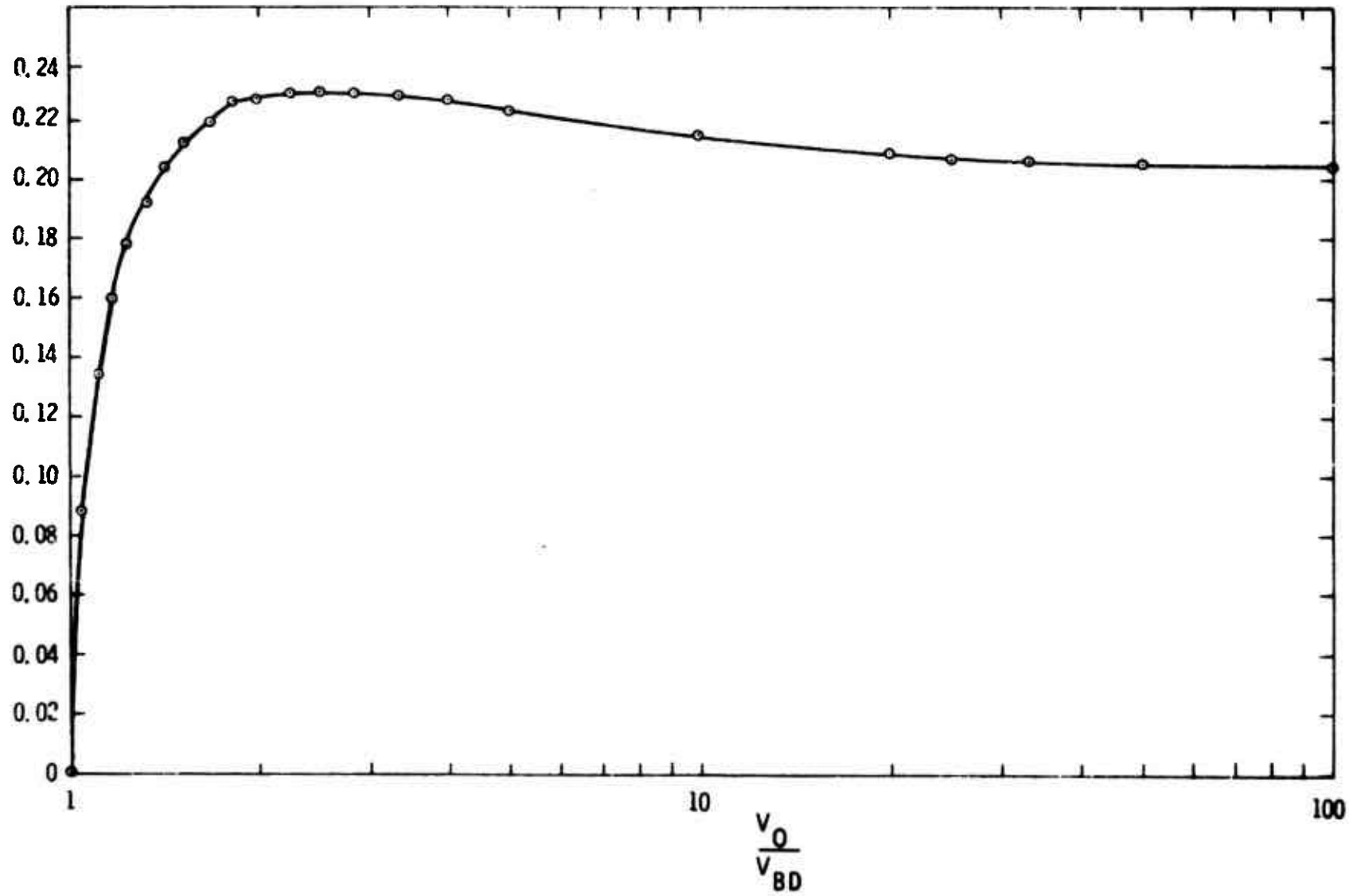


Figure B-4. Plot of t_p/t_s Versus V_0/V_{BD}

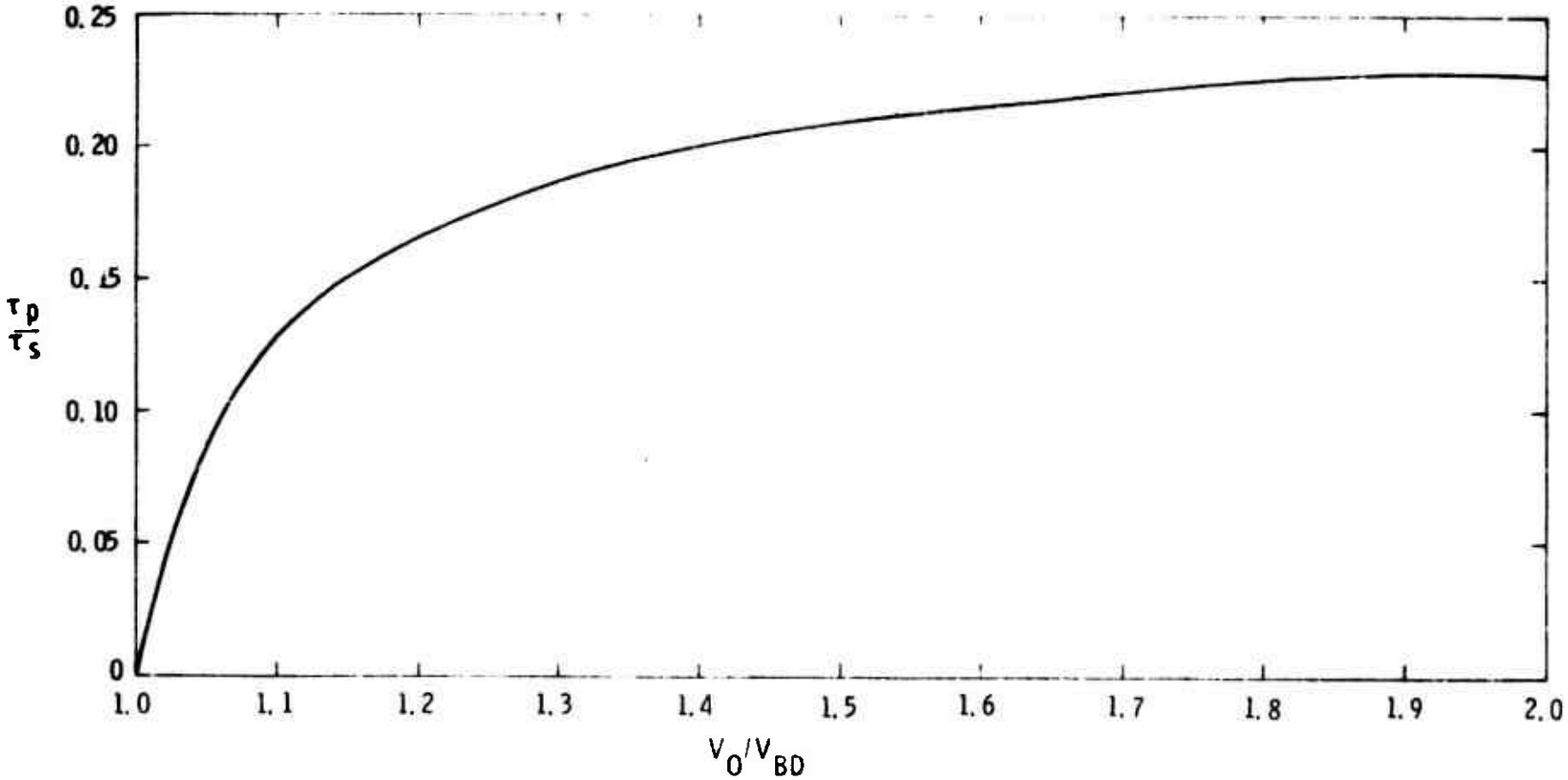


Figure B-5. Plot of τ_p/τ_s Versus V_0/V_{BD} for Values of V_0/V_{BD} Less Than 2

APPENDIX C

ELECTRONIC CIRCUIT ANALYSIS AND DESIGN BY DRIVING-POINT IMPEDANCE TECHNIQUES

Electronic Circuit Analysis and Design by Driving-Point Impedance Techniques

RUBEN D. KELLY

Abstract—By using driving point impedance (DPI) techniques a systematic approach to the analysis of electronic circuits can be developed which helps the engineer gain insight into circuit action. The answers, representing the circuit's currents, voltages, gains, and driving-point impedances, are written down by inspection of the original circuit diagram without resorting to equivalent circuits of flow graphs. The resulting answers are in a most simple form which can be easily interpreted by inexperienced persons since the relative magnitude of each factor is known. Thus, the student rapidly obtains a "feel" for electronic circuits. The method can also be used to complement a computer-aided circuit design and analysis.

A tutorial treatment of the fundamental methods is presented and two examples are given. The simple example, which is complex by ordinary standards, has five input signals and three active elements; yet the output signal voltage is written out by inspection with each step explained.

The second example, a two-stage transistor feedback amplifier, is used to demonstrate how the fundamental concepts are applied to complex feedback circuits. The gain, input impedance, and output impedance of the feedback amplifier are found and approximations are used to compare the answers to ordinary solutions given for such amplifiers. The answers obtained by DPI analysis methods are also compared to equivalent answers found by node analysis.

Introduction

SOON after the advent of the transistor, it became apparent that a new method of teaching electronics would be required if a teacher hoped to keep his students abreast with the myriad of new electron devices and circuits. Most every electroniker[1] had developed his own methods so that he had a "feel" for electronic circuits. Many teachers had used Thevenin's theorem to reduce a circuit to a single equivalent impedance and single equivalent voltage in order to explain more simply the concepts of frequency and transient response. Thevenin's theorem also was used to simplify the concept of one circuit loading or interacting with another. With no systematic circuit analysis techniques available except loop and node analysis, the average person found it difficult to develop a feel for the electronic circuit, especially if it was very complex.

A new systematic electronic circuit analysis and design technique, designated driving-point impedance (DPI) analysis, has been developed by the author for use in teaching electronics at the University of New Mexico. By using a few fundamental circuit concepts, which the average student can easily master, one can in a very short period of time become proficient in the analysis of the most complex circuits and develop, as one student so vividly described it, a "gut feeling" for electronic circuits. DPI analysis allows the student to write out answers to complex circuits by inspection, and because the answers are products and/or sums of simple terms, the student rapidly learns how to approximate answers.

Two years ago, Kirtland Air Force Base (KAFB), under a special services contract, employed the author to teach a 25-lecture beginning course in electronic circuit analysis and design using DPI analysis techniques. The beginning course was so successful that a second more advanced course was offered the next semester. Since that time both the beginning and advanced course have been repeated. The classes at KAFB consisted of students who are electrical engineers, technicians, and nonelectrical engineers. Although there were excellent students in each category, some of the best students were technicians and nonelectrical engineers, which indicates that DPI analysis can be mastered by anyone interested in electronics. KAFB personnel have found DPI analysis to be very valuable, especially as an aid in complementing computer analysis of electronic circuits. In the following paragraphs the basic concepts of DPI analysis will be explained and a feedback amplifier will be analyzed to demonstrate the capabilities of the DPI analysis technique.

The current-divider equation and the voltage-divider equation are indispensable for the analysis of electronic circuits by the DPI method. Referring to Fig. 1, it is noted that the output voltage appears across the parallel combination of R_2 and R_3. In order to maintain simplicity of answers the equivalent resistance represented by the parallel combination of R_2 and R_3 will be denoted by the shorthand notation $(R_2 \| R_3)$. The magnitude of $(R_2 \| R_3)$ can be determined as the product divided by the sum; thus, $(R_2 \| R_3) = (R_2 R_3)/(R_2 + R_3)$. The shorthand notation is extended if more than two resistances are in parallel; for example, the parallel combination of the three resistors R_x, R_y, and R_z is denoted as $(R_x \| R_y \| R_z)$; however, the magnitude of $(R_x \| R_y \| R_z)$ can be best calculated by taking two resistances at a time and utilizing the product divided by the sum (which

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[1] An electroniker is an individual capable of analyzing, designing, and constructing electronic circuitry.

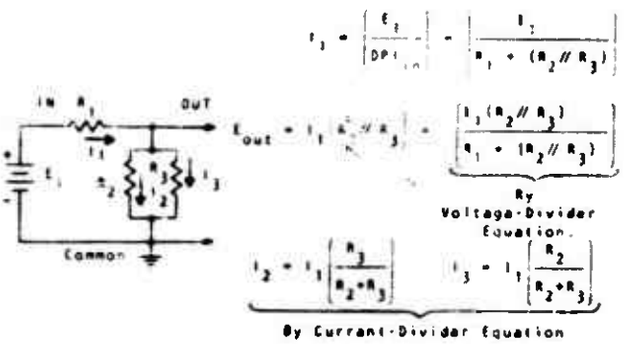


Fig. 1. Series-parallel circuit demonstrating voltage-divider and current-divider equations.

applies to only two resistors in parallel); thus, $(R_x \| R_y \| R_z) = (R_x \| R_y) \| (R_z)$. First, calculate $(R_x \| R_y) = R_{eq}$; then find $R_{eq} \| R_z$.

Making use of the shorthand notation for parallel resistors, the current supplied by E_1 for the circuit shown in Fig. 1 is

$$I_1 = \frac{E_1}{\mathrm{DPI}_{in}} = \frac{E_1}{R_1 + (R_2 \| R_3)} \tag{1}$$

The output voltage E_{out} is the Ohm's law voltage drop across $(R_2 \| R_3)$ caused by I_1; thus

$$E_{out} = I_1(R_2 \| R_3) = E_1\left[\frac{(R_2 \| R_3)}{R_1 + (R_2 \| R_3)}\right]. \tag{2}$$

The latter form of the E_{out} expression given by (2) is designated as the voltage-divider equation. It can be interpreted as follows. In a series circuit, the voltage across any series element is found by multiplying the applied voltage by the value of the particular series element (across whose terminals the voltage drop is desired) and dividing the result by the summation of all the series elements. Using shorthand notation for parallel elements simplifies the appearance (and interpretation) of the resulting equation.

Referring back to Fig. 1, it is noted that the total current I_1 was easily found by dividing E_1 by the DPI_{in} as seen from the E_1 viewpoint. With the value of I_1 known, it is desired to determine the current flowing through each of the parallel resistors I_2 and I_3. The currents through each member of a parallel branch can be derived for each problem, but a simple current-divider expression can be found which will apply to all cases. The current-divider equation is derived as follows. The voltage across R_2 and R_3 is $I_1 (R_2 \| R_3)$. The current I_2 flowing through R_2 is found by Ohm's law as [the voltage across $(R_2 \| R_3)$] divided by (R_2), yielding

$$I_2 = \frac{I_1(R_2 \| R_3)}{R_2} = \left[I_1\left[\frac{R_2 R_3}{R_2 + R_3}\right]\right]\left[\frac{1}{R_2}\right]$$

$$= I_1\left[\frac{R_3}{R_2 + R_3}\right]. \tag{3}$$

The latter expression for I_2 given in (3) is known as the current-divider equation. It may be interpreted as follows. The current through a particular element of a two-resistor parallel combination is found by multiplying the total current entering the node by the value of the opposite resistance and then dividing the result by the sum of the two resistances. If more than two elements are in parallel interpret the opposite resistance to mean the parallel combination of all elements except the one through which the current is desired. For example, if I_T is flowing into the parallel combination of three resistors R_x, R_y, and R_z, and it is desired to find I_x, the result is

$$I_x = I_T\left[\frac{(R_y \| R_z)}{R_x + (R_y \| R_z)}\right] \quad \text{equivalent opposite resistance.} \tag{4}$$

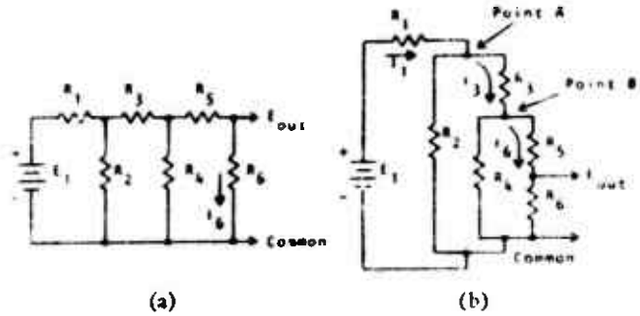
Using the current-divider equation, the current I_3 in Fig. 1 is easily obtained as

$$I_3 = I_1\left[\frac{R_2}{R_2 + R_3}\right]. \tag{5}$$

One more simple example will be cited to demonstrate the simplicity of the method. The expression for E_{out} in Fig. 2 is seen to be $I_6 R_6$ by Ohm's law voltage drop. The current I_6 can be found by first writing I_1 as $(E_1 / \mathrm{DPI}_{in})$ and then applying the current-divider equation at the R_2–R_3 node to find I_3, and again applying the current-divider equation at the R_5–R_6 node to find I_6. The result of E_{out} found by employing the current-divider equation is

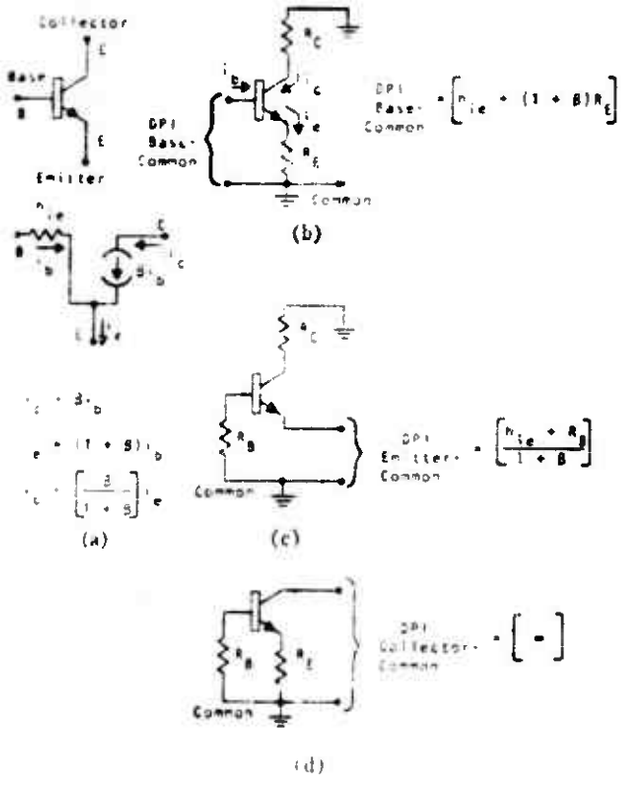
$$E_{out} = I_6 R_6 = \underbrace{\left[\frac{E_1}{R_1 + (R_2) \| [R_3 + (R_4) \| (R_5 + R_6)]}\right]}_{I_1}\underbrace{\left[\frac{R_2}{R_2 + [R_3 + (R_4) \| (R_5 + R_6)]}\right]}_{I_3}\underbrace{\left[\frac{R_4}{R_4 + R_5 + R_6}\right]}_{I_5 = I_6}(R_6). \tag{6}$$

The voltage E_{out} in Fig. 2 can be written out just as easily by utilizing the voltage-divider equation. The voltage at point A can first be obtained by applying the voltage-divider equation to E_1, R_1, and the remainder of the circuit. With the voltage at point A known, the



(a) (b)

Fig. 2. Circuit for finding E_{out} by the current-divider and/or the voltage-divider technique.



(a) (b) (c) (d)

Fig. 3. Bipolar transistor characteristics (current-controlled current source). (a) Symbols, equivalent circuit, and current relationships. (b) Base DPI. (c) Emitter DPI. (d) Collector DPI.

voltage at point B can be obtained by applying the voltage-divider equation to V_A and the circuit branch from point A to point B. Finally, the voltage E_{out} is obtained by once again applying the voltage-divider equation to the voltage V_B and the R_5-R_6 divider circuit. The result written out by inspection in one step is as follows:

$$I_{out} = I_1 \underbrace{\left[\frac{(R_2)\,[R_3 + (R_4)\,(R_5 + R_6)]}{R_1 + (R_2)\,[R_3 + (R_4)\,(R_5 + R_6)]}\right]}_{\text{voltage-divider; } E_1 \text{ to point } A} \underbrace{\left[\frac{(R_4)\,(R_5 + R_6)}{R_3 + (R_4)\,(R_5 + R_6)}\right]}_{\text{voltage-divider; point } A \text{ to point } B} \underbrace{\left[\frac{R_6}{R_5 + R_6}\right]}_{\text{voltage-divider; point } B \text{ to output}} \tag{7}$$

voltage at point A

voltage at point B

The above two answers given in (6) and (7) for E_{out} are exactly equivalent and each was written out by inspection. If the circuit contains more than one voltage source, the answer can still be written out by inspection by applying superposition; that is, considering each voltage individually while letting the remaining voltages be zero and algebraically adding the results (contributions) of each voltage to obtain a total result.

The preceding discussion of the circuits in Fig. 1 and Fig. 2 illustrates the methods used to write out the currents and voltages in a multiloop circuit. We need now only to know the simple DPI of basic electronic circuits so that these terms can be used to write out by inspection the answers to multistage amplifiers, including those that contain feedback.

When active devices such as transistors and vacuum tubes are employed in electronic circuits, the DPI at various nodes in the circuit are modified by the action of the dependent controlled sources. Three basic types of controlled sources appear in the three most commonly used active circuit elements. The common bipolar transistor shown in Fig. 3 exhibits a current-controlled current source; the field effect transistor (FET) shown in Fig. 4 exhibits a voltage-controlled current source; whereas, the triode vacuum tube shown in Fig. 5 exhibits a voltage-controlled voltage source.

By knowing the DPI at each electrode relative to the common connection of the other two terminals, how gate voltage controls drain current in an FET, and how grid voltage controls plate current in a tube, it is possible to use Ohm's and Kirchhoff's laws to write out the solution to the most complex of circuits by inspection. Before proceeding it should be pointed out that the solution to circuit currents and voltages can also be written out by inspection using loop and/or node analy-

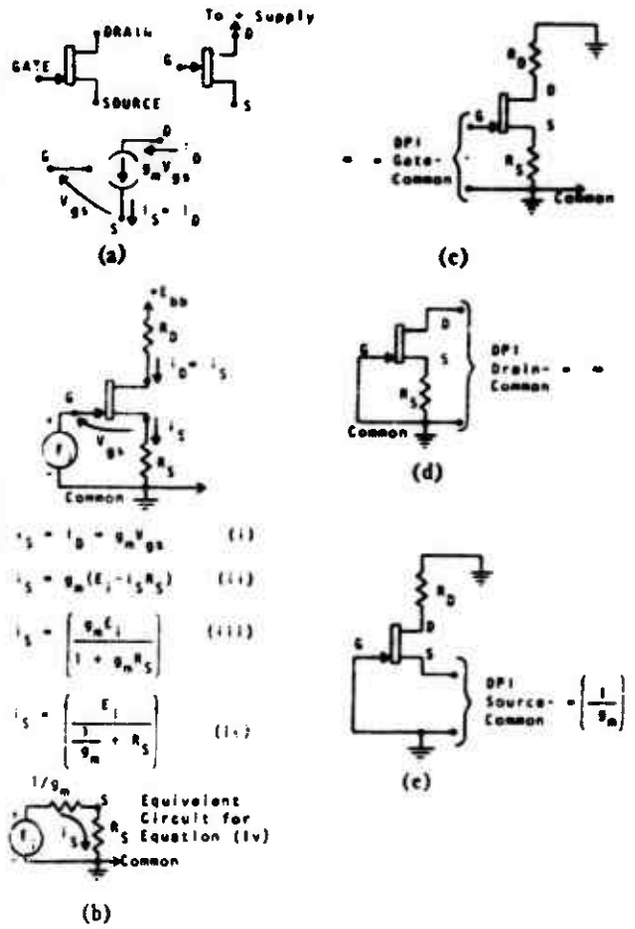


Fig. 4. Field effect transistor characteristics (voltage-controlled current source). (a) Symbols and equivalent circuit (neglecting r_{ds}). (b) Drain current ($i_D = i_S$) as a function of E_i applied between gate and common. (c) Gate DPI. (d) Drain DPI. (e) Source DPI.

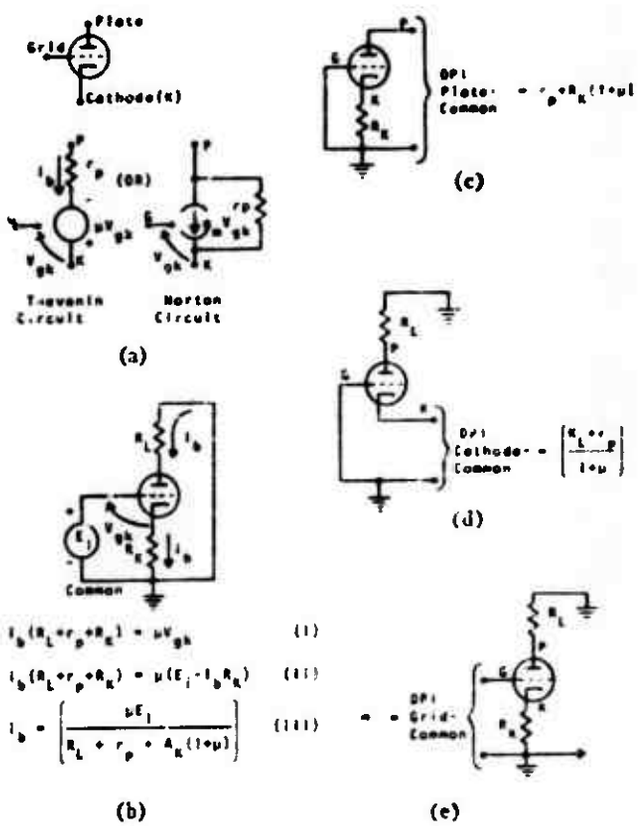


Fig. 5. Triode vacuum tube characteristics (voltage-controlled voltage source). (a) Symbol and equivalent circuit. (b) Plate current as a function of E_i applied between grid and common. (c) Plate DPI. (d) Cathode DPI. (e) Grid DPI.

sis methods; however, the results of node and loop analysis are not easily comprehended because the answer is in the form of the ratio of two n-by-n determinates. On the other hand, the result of the DPI analysis is in the form of products and sums of simple voltage-divider, current-divider, or Ohm's law expressions, each of which is easy to comprehend and/or visualize by the average person.

Common Bipolar Transistor

Referring to Fig. 3(a) we note that the base current i_b controls the βi_b current generator in the collector circuit. Thus, the i_b base current and the βi_b collector current combine at the emitter node to make emitter current $i_e = i_b(1+\beta)$. In Fig. 3(b), the action of the controlled source for a given i_b causes the base voltage to be $v_b = i_b h_{ie} + i_b(1+\beta)R_E$. Since this causes the v_b voltage to increase at an $i_b[h_{ie}+(1+\beta)R_E]$ rate, the base DPI is $[h_{ie}+(1+\beta)R_E]$. Thus, the βi_b controlled source causes the emitter resistor R_E to appear $(1+\beta)$ times larger from the base-circuit viewpoint.

In Fig. 3(c) the DPI seen at the emitter is $(h_{ie}+R_B)/(1+\beta)$. This implies that a voltage V_E applied to the emitter will supply a current as though it were connected to an impedance of $(h_{ie}+R_B)/(1+\beta)$. The circuit action that causes $(h_{ie}+R_B)$ to appear $(1+\beta)$ times smaller is a result of the controlled (dependent) βi_b generator. With V_E applied directly to the emitter, $(h_{ie}+R_B)$ will be directly across its terminals and a current will flow in the base circuit equal to $(V_E)/(h_{ie}+R_b)$, but this base current excites the βi_b generator and causes additional current of βi_b to be supplied by V_E. The result of this increased current flow is that $(h_{ie}+R_B)$ appears to be smaller from the emitter circuit viewpoint by a $(1+\beta)$ factor; thus, the DPI at the emitter is $(R_B+h_{ie})/(1+\beta)$.

In Fig. 3 (d) it is noted that the DPI seen looking into the collector is infinity if the base and emitter are referenced to common. This results from the fact that the βi_b generator can only be excited by signals in the base-emitter loop, and since a voltage applied only to the collector cannot excite a current in the base circuit, the βi_b current generator is independent (not excited) and appears as an infinite DPI, a characteristic of all independent current generators.

Field-Effect Transistor

Referring to Fig. 4(a) it is noted that there are conflicting symbols for the junction FET. When the gate arrow is colinear with the source terminal, there is no

ambiguity as to which are the source and drain terminals; however, when the gate arrow is midway between the source and drain terminals[2] it is necessary to trace the circuit to see which terminal is connected to the power supply. For n-channel FET's as illustrated, the terminal returned to the (+) power supply is the drain. For p-channel FET's the gate arrow direction is opposite and the drain terminal must be connected to a (−) power supply. DPI analysis applies exactly the same to either n-channel or p-channel FET's. It should be noted that DPI analysis as described in Fig. 3 applies exactly the same to either n-p-n or p-n-p bipolar transistors

The derivation given in Fig. 4(b) shows that the source and drain currents are equal (the gate draws zero current) and that source current i_s as caused by E_i on the gate relative to common can be calculated as though E_i were forcing current through the series combination $[(1/g_m)+R_s]$, although the actual E_i generator supplies zero current to the gate. This apparent circuit action, resulting from the controlled (dependent) current source $(g_m V_{gs})$, is helpful in calculating source current without deriving the equation each time. Thus, any E_i applied to the gate relative to ground causes a source and drain current of $i_s = i_d = (E_i)/[(1/g_m)+R_s]$. The source voltage is the $i_s R_s$ voltage drop and is that portion of the voltage appearing across R_s in the two-resistance voltage divider equivalent circuit that represents equation (iv) in Fig. 4(b). As shown in Fig. 4(e), the $1/g_m$ term represents the DPI at the source.

Since the E_i signal applied to the gate supplies zero current, the DPI at the gate is infinite as illustrated in Fig. 4(c). The DPI seen looking in on the drain [see Fig. 4(d)] is also infinite because application of a voltage to only the drain cannot excite the $g_m V_{gs}$ generator and the DPI of an independent current generator is infinite.

The DPI seen looking in at the source, Fig. 4(e), is $(1/g_m)$. If an external voltage V_s were applied to the source in Fig. 4(e), it would supply a current equal to $(V_s)/(1/g_m)$ because the V_s voltage is directly between the source and the gate terminals and it excites the $g_m V_{gs}$ current generator and causes V_s to supply a current of $g_m V_{gs}$. This circuit action makes the source DPI equal to $(1/g_m)$.

Triode Vacuum Tube

In order to complete our list of dependent-source types we will include the triode vacuum tube whose equivalent circuit exhibits a voltage-controlled voltage source. Ironically, the analysis of the vacuum tube circuit is returning to prominence because its DPI equations can be used to analyze an FET amplifier which has a resistance r_{ds} between drain and source (paralleling the $g_m V_{gs}$ generator) that cannot be neglected.[3] Referring to Fig. 5(a), it is noted that the FET equivalent circuit is identical in the tube's Norton equivalent circuit if $r_p = \infty$. In fact, if all the vacuum tube DPI equations are taken to the limit as $r_p \to \infty$ and $(\mu/r_p) \to g_m$, they will become exactly the same as the FET DPI equations.

For the vacuum tube, one needs to know the following three things: 1) the plate current resulting from E_i being applied between the grid and common given in Fig. 5(b) as $i_b = (\mu E_i)/[R_L + r_p + R_K(1+\mu)]$; 2) the DPI seen looking in at the plate relative to common given in Fig. 5(c) by the expression $[r_p + R_K(1+\mu)]$, which implies that any impedance in the cathode lead that is in both the plate loop and the grid-cathode loop will appear $(1+\mu)$ times larger from the plate circuit's viewpoint; 3) the DPI seen looking into the cathode relative to common given in Fig. 5(d) as $(R_L + r_p)/(1+\mu)$, which means that any impedance in the plate lead will appear $(1+\mu)$ times smaller from the cathode circuit viewpoint.

Simple Nonfeedback Example

A straightforward example of the use of the DPI analysis technique is presented in Fig. 6. Superposition is used to write out the E_{out} contribution due to each signal source. The base DPI is used to obtain base current due to E_1 which is then multiplied by $(1+\beta)$ to obtain emitter current. A current-divider equation is used to find the portion of emitter current which flows into the FET source (which is also drain current). Another current-divider equation is employed to determine how much drain current (resulting from E_1) flows into the cathode of the tube. Since the signal current caused by E_1 flows up through R_L, it will produce a (+) output voltage contribution.

The source and drain currents excited by E_2 are calculated using equation (iv) in Fig. 4(b) where the equivalent source load is $(R_{FS}) \| [R_B + h_{ie}/(1+\beta)]$. The drain current excited by E_2 divides between R_K and the cathode DPI of the tube; a current-divider equation is used to determine the tube's portion. Since the plate current caused by E_2 flows down through R_L, the polarity of its contribution to E_{out} is negative (−).

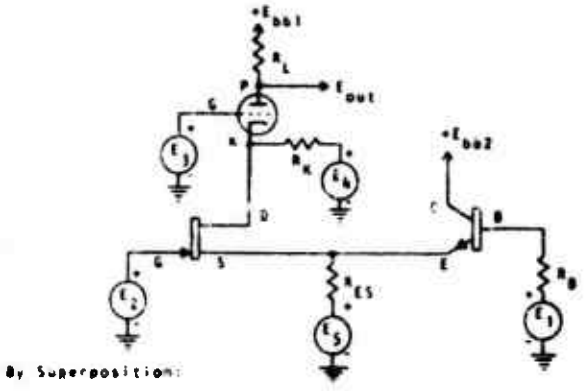
The plate current excited by E_3 is calculated by using equation (iii) in Fig. 5(b) where the cathode load is

[1] The last symbol is preferred by the author because one can tell immediately which terminals correspond to the source and the drain; however, many authors prefer the latter symbol since it more appropriately represents the symmetrical nature of the FET structure, whereby for many FET's the two extreme terminals are interchangeable, and the additional circuit tracing described previously is required to determine which electrodes are being used as the drain and the source.

[3] If r_{ds} is given, it can be neglected when it is large compared to the DPI seen between source and drain; that is,

$$r_{ds} \gg (R_D + R_S) \left\| \left[\frac{1}{g_m \left[\frac{R_S}{R_S + R_D} \right]} \right] \right.$$

for the circuit in Fig. 4(b).



By Superposition:

$$E_{out} = +\left[\frac{E_1}{R_B + r_\pi + (1+\beta)(R_{ES} /\!/ \frac{1}{g_m})}\right](1+\beta)\left[\frac{R_{ES}}{R_{ES} + \frac{1}{g_m}}\right]\left[\frac{R_K}{R_K + \left[\frac{R_L + r_p}{1+\mu}\right]}\right](R_L)$$

$$- \left[\frac{E_2}{\frac{1}{g_m} + \left[R_{ES} /\!/ \frac{R_B + r_\pi}{1+\beta}\right]}\right]\left[\frac{R_K}{R_K + \left[\frac{R_L + r_p}{1+\mu}\right]}\right](R_L)$$

$$- \left[\frac{+E_3}{R_L + r_p + (1+\mu)R_K}\right](R_L) + \left[\frac{E_4}{R_K + \left[\frac{R_L + r_p}{1+\mu}\right]}\right](R_L)$$

$$+ \left[\frac{E_5}{R_{ES} + \left[\frac{1}{g_m} /\!/ \frac{R_B + r_\pi}{1+\beta}\right]}\right]\left[\frac{\left[\frac{R_B + r_\pi}{1+\beta}\right]}{\left[\frac{R_B + r_\pi}{1+\beta}\right] + \frac{1}{g_m}}\right]\left[\frac{R_K}{R_K + \left[\frac{R_L + r_p}{1+\mu}\right]}\right](R_L)$$

Fig. 6 DPI example problem

$[(R_K)\|(\text{Drain DPI})] = [R_K]$. The plate current due to E_3 flows down through R_L and causes a negative (−) contribution to E_{out}.

The value of plate current due to E_4 is obtained by dividing E_4 by R_K plus the cathode DPI (the drain DPI is infinite), and since this current flows up thrnugh R_L it causes a (+) positive contribution to E_{out}.

The current from E_5 flows up through R_{ES} and splits between the FET source and the emitter. The portion through the FET source is also drain current and it splits between R_K and the cathode DPI. Since it flnws up through R_L, it causes a (+) contribution to E_{out}.

In addition to the E_{out} signal, the DPI_{out} is always required. The ontput DPI at the tube's plate is $R_L\|[r_p + R_K(1+\mu)]$.

Two-Stage Feedback Amplifier

The following problem appeared on the final exam at KAFB in the fall nf 1969, and is used here as an example nf how to analyze feedback amplifiers.

The two-stage feedback amplifier shown in Fig. 7 is to be analyzed for DPI_{in}, DPI_{out}, and gain.

It is noted that the DPI_{in} consists of R_i in series with

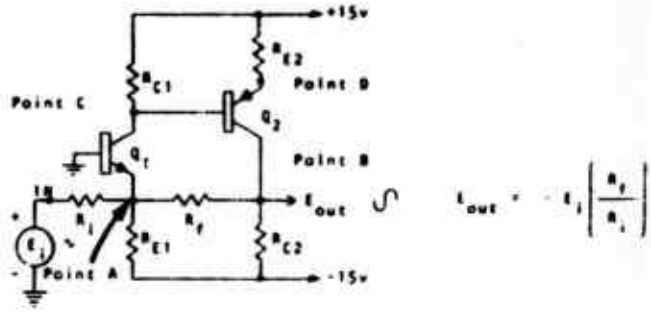


Fig. 7. A two-stage feedback amplifier.

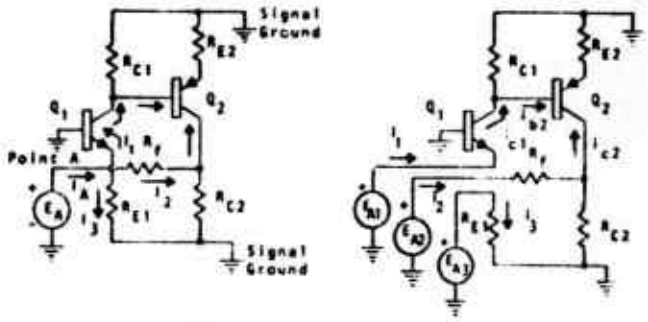


Fig. 8. Circuit diagram for finding the DPI at point A.

the DPI seen at point A from the R_i viewpoint; therefore, the analysis will proceed by moving over to point A and deriving the $DPI_{point\ A}$.

In order to take advantage of the DPI analysis techniques, we will determine the current drawn from a voltage E_A applied at point A, and once the current is known, the $DPI_{point\ A} = (E_A)/(I_{A\ total})$. The solution never need be carried to completion because the superposition sum of currents implies several equivalent impedances in parallel and from this sum of currents one can write out the DPI by inspection using the shorthand notation for parallel resistances.

Referring to Fig. 8(a) it is noted that the circuit has been drawn with an independent voltage E_A driving point A. Because E_A excites an emitter current in Q_1, and the resulting collector current of Q_1 excites a base current in Q_2 which causes the collector current of Q_2 to produce a current flnw in R_f, it is always advisable to draw a separate E_A generator for each circuit branch connected to point A so that one may easily keep track of every current. The circuit is redrawn in Fig. 8(b) with voltage sources E_{A1}, E_{A2}, and E_{A3} connected, respectively, to the emitter nf Q_1, to resistor R_f, and to resistor R_{E1}. Failure to draw a separate generator for each circuit branch often leads to the overlooking of one or more of the superposition currents. In nrder to keep from overlooking any of the currents, each nf the three vnltages is considered individually while the remaining two are set equal to zero; in other words, superposition is applied. As each voltage is considered, the current in its own branch and the currents

which it might excite in the other two branches are algebraically combined by considering currents into a branch positive (+) while considering currents coming out of a branch negative (−). By tracing currents through the circuit of Fig. 8(b) it is easy to show that E_{A1} causes a Q_1 emitter current in its own branch and a current into R_f in the E_{A2} branch; however, it does not excite a current in the E_{A3} branch. On the other hand, E_{A3} excites a current only in its own branch of R_f and R_{C2}, while E_{A2} causes a current only in R_{E1}. Each of the currents described can be written out by inspection, and the results can be summed algebraically by superposition when we let $(E_{A1} = E_{A2} = E_{A3}) = E_A$.

Referring to Fig. 8(b), we note that the total currents excited by E_{A1} in each of the three branches can be denoted as

$$i_1 = i_1(E_{A1}) + i_2(E_{A1}) + i_3(E_{A1}) \tag{8}$$

where $i_1(E_{A1})$ is the emitter-1 current due to E_{A1}, $i_2(E_{A1})$ is the current in R_f caused by E_{A1}, and $i_2(E_{A1})$ is the current in R_{E1} caused by E_{A1}.

Using the current-divider equation and the DPI equations for the bipolar transistor given in Fig. 3, we may write out i_1 total by inspection as follows:

$$i_1 = \frac{E_{A1}}{\left[\frac{h_{ie1}}{1+\beta_1}\right]} + \frac{E_{A1}}{\left[\frac{h_{ie1}}{1+\beta_1}\right]} \left\{\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)\left[\frac{R_{C2}}{R_{C2}+R_f}\right]\right\} + \text{zero} \tag{9}$$

(i_1 into emitter-1; gives i_{c1}; I-divider gives i_{b2}; gives i_{c2}; I-divider gives i_f; current through R_f excited by E_{A1})

Note that emitter-1 current is common in the first two terms and will be factored out in the final expression. The current in R_f excited by E_{A1}, the second term in (9), is found by multiplying the emitter current of Q_1 by $(\beta_1)/(1+\beta_1)$ to obtain Q_1 collector current i_{C1}; multiplying this Q_1 collector current by the current-divider equation of R_{C1} and the base DPI of Q_2 to obtain base current in Q_2, multiplying the resulting i_{b2} current by (β_2) to obtain the Q_2 collector current i_{C2}, and finally multiplying i_{C2} by the current-divider equation of R_f and R_{C2} to obtain the current in R_f. The polarity of this R_f current due to E_{A1} is positive (+) since it flows into the R_f branch.

Referring again to Fig. 8(b) the current i_2 due to E_{A2} can be represented by

$$i_2 = i_1(E_{A2}) + i_2(E_{A2}) + i_3(E_{A2}) \tag{10}$$

where $i_1(E_{A2})$ is the emitter-1 current due to E_{A2}, $i_2(E_{A2})$ is the current in R_f caused by E_{A2}, and $i_3(E_{A2})$ is the current in R_{E1} caused by E_{A2}.

It can be noted that E_{A2} cannot excite a current in the collector of Q_2 through R_f since the DPI of Q_2's collector is infinite, and therefore, E_{A2} cannot possibly excite an emitter current in Q_1. Also, E_{A2} cannot excite a current in R_{E1}; consequently, $i_1(E_{A2})$ and $i_3(E_{A2})$ are both zero. The current i_2 can be written out by inspection as

$$i_2 = \text{zero} + \frac{E_{A2}}{R_f + R_{C2}} + \text{zero} \tag{11}$$

where the second term representing $i_2(E_{A2})$ represents E_{A2} forcing current through the series combination of R_f and R_{C2} (because the Q_2 collector DPI is infinite from the E_{A2}–R_f viewpoint).

The voltage E_{A2} can excite current only in R_{E1}. Therefore, the expression for the current i_2 becomes

$$i_2 = i_1(E_{A2}) + i_2(E_{A2}) + i_3(E_{A2}) \tag{12}$$

$$i_2 = \text{zero} + \text{zero} + \frac{E_{A2}}{R_{E1}}. \tag{13}$$

But $(E_{A1} = E_{A2} = E_{A3}) = E_A$ and $I_A = i_1 + i_2 + i_3$; therefore, the expression for the total current I_A becomes

$$I_A = \left\{\frac{E_{A1}}{\left[\frac{h_{ie1}}{1+\beta_1}\right]}\left[1 + \left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)\left[\frac{R_{C2}}{R_{C2}+R_f}\right]\right] + \frac{E_{A2}}{(R_f + R_{C2})} + \frac{E_{A3}}{(R_{E1})}\right\} \tag{14}$$

and since I_A is in the form $I_A = E_A[(1/R_x) + (1/R_y) + (1/R_z)] = E_A/(R_x \| R_y \| R_z) = E/(\text{DPI}_{\text{point } A})$, we may write out by inspection,

$$\mathrm{DPI}_{in} = R_i + \mathrm{DPI}_{\text{point } A} \tag{15}$$

$$= R_i + \underbrace{\left\{ \frac{\left[\frac{h_{ie1}}{1+\beta_1}\right]}{1 + \left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie1} + (1+\beta_2)R_{E1}}\right](\beta_2)\left[\frac{R_{C2}}{R_{C2}+R_f}\right]} \right\} \| (R_f + R_{C2}) \| (R_{E1})}_{\text{this is the factor which makes } \mathrm{DPI}_{\text{point } A} \text{ such a low impedance}} \tag{16}$$

Before proceeding to the calculations for gain and DPI_{out} it will be beneficial to describe how these two answers can be found. Referring back to the original schematic shown in Fig. 7, it is noted that the feedback through R_f from the E_{out} terminal is the only thing that prevents us from using the standard current-divider equation at point A; that is, the voltage at the E_{out} terminal modifies the current division at point A because the feedback modifies the DPI at point A. In the previous analysis for DPI_{in}, we could not write out the answer from the input terminal viewpoint because the output voltage feeds back through R_f and modifies the potential at point A and also the current division there. In other words, the potential at point A is not known unless you solve the entire problem; it is a summing junction for the input and output circuits. However, when we moved over to point A and applied a voltage source of E_A at this summing junction, we prevented the output voltage from controlling the potential at point A; that is, E_A killed the feedback voltage; point A potential was fixed by E_A. Once we had disabled feedback voltage variations at point A we could use standard current-divider equations and superposition to write out answers.

In order to kill feedback in the original circuit of Fig. 7, we can apply a voltage E_x to the output terminal to fix the output voltage to the value E_x which is independent of feedback. The circuit with both E_i and E_x applied is shown in Fig. 9.

It is noted in Fig. 9 that if superposition is used the current division at point A is known by standard current-divider equations for either E_i or E_x considered individually while letting the remaining voltage be set equal to zero. That is, when E_x = zero, the current division at point A is known since the output is shorted to ground and no feedback voltage occurs. Likewise, when E_i = zero, the current division at point A due to E_x excitation is known by standard current-divider equations since the input terminal is shorted to ground. The total current in any branch of the circuit is the superposition sum of the currents due to E_x and the currents due to E_i with each set of currents calculated by standard DPI methods. Thus, the purpose of E_x is to disable or kill feedback so that standard DPI analysis can be used throughout the circuit.

The total current I_x shown on the circuit diagram in

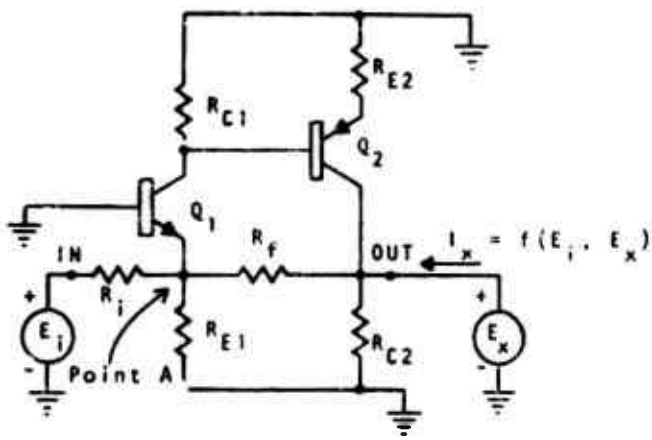


Fig. 9. Feedback amplifier with E_x connected to output terminal.

Fig. 9 is a superposition sum of the individual currents caused by E_i and E_x independently, and these currents can be written out by inspection using DPI analysis methods. The most important concept, however, is that if E_x were disconnected from the output terminal, the E_{out} voltage appearing at the output would be that of the complete feedback amplifier when E_i is the input signal, and if E_x were adjusted to be identically equal to the E_{out} existing with feedback, and then $E_x \equiv E_{out}$ (with feedback) reconnected to the output terminal, the current $I_x = f(E_i, E_x)$ would be identically zero. This concept is used to determine what value of E_x will be required to make $I_x = f(E_i, E_x)$ identically zero, and of course this particular value of E_x is also the value of E_{out} with feedback. The concept is simple and the writing out of $I_x = f(E_i, E_x)$ by superposition using DPI analysis is also simple; in fact, the final analysis is shortened considerably more by noting what the concept implies.

In using the concept, it is noted that $I_x = f(E_i, E_x = 0)$ is really short-circuit output current (I_{sc}) and that the I_x current due to E_x only is $I_x = f(E_i = 0, E_x) = (E_x/\mathrm{DPI}_{out})$. Thus, when the total I_x is found it is of the form

$$I_x = I_x(E_i, E_x = 0) + I_x(E_i = 0, E_x) \tag{17}$$

$$I_x = -I_{sc} + \frac{E_x}{\mathrm{DPI}_{out}}. \tag{18}$$

The short-circuit current I_{sc} is considered negative in

(18) because it is coming out of the circuit, whereas the I_s direction was considered into the circuit.

Setting I_s identically equal to zero as required by the concept stated previously, we obtain

$$0 = -I_{SC} + \frac{E_s}{\mathrm{DPI_{out}}} \tag{19}$$

and solving for E_s

$$E_s = (I_{SC})(\mathrm{DPI_{out}}) = E_{out} \quad \text{with feedback.} \tag{20}$$

More importantly, it should be noted that $E_{out} = (\text{gain})(E_i)$ and that if (20) is divided by E_i we will obtain the circuit gain; one of the requirements of the initial problem. Thus, utilization of the above concept of applying E_s and setting $I_s = 0$ yields both the gain and the $\mathrm{DPI_{out}}$ simultaneously which is perhaps why the students prefer this method of analyzing feedback amplifiers.

As mentioned above, the obtaining of the results given by (20) is considerably shortened by noting that only the $\mathrm{DPI_{out}}$ as determined by E_s acting alone, and the I_{SC} due to E_i acting alone, is all that is required; that is, one never has to go through all the steps to get the results of (20). Short-circuit current $I_{SC} = I_s(E_i,\ E_s = 0)$ is required of course, but when $I_s = f(E_i = 0,\ E_s)$ is being calculated, it is noted that it is of the form $(E_s)[(1/R_a) + (1/R_b) + (1/R_c)] = (E_s)/(R_a \| R_b \| R_c) = (E_s)/(\mathrm{DPI_{out}})$ so that it is never necessary to carry the calculations beyond the initial step in order to obtain $\mathrm{DPI_{out}}$ since it is noted from the initial form of $I_s = E_s[(1/R_a) + (1/R_b) + (1/R_c)]$ that $\mathrm{DPI_{out}} = (R_a \| R_b \| R_c)$.

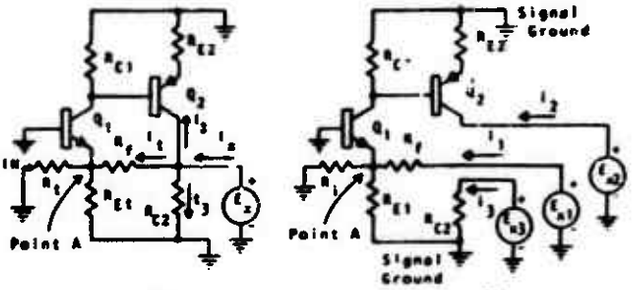


Fig. 10. Circuit for calculating the output DPI of feedback amplifier.

Proceeding with the original problem, we calculate the current $I_s = f(E_i = 0,\ E_s)$ by using the circuit diagram shown in Fig. 10. E_i is set equal to zero which shorts the input to ground, and E_s is assumed to drive the output terminal, Fig. 10(a). The circuit is redrawn in Fig. 10(b) with E_{s1}, E_{s2}, and E_{s3} connected, respectively, to resistor R_f, to the collector of Q_2, and to resistor R_{C2}. The current i_1 from E_{s1} enters the node at point A and excites emitter current in Q_2 which in turn excites base current in Q_2 and causes Q_2 collector current to flow in the E_{s2} circuit. E_{s1} acting alone cannot excite any currents since it is working into the infinite DPI of Q_2's collector; therefore, $i_2 = f(E_{s2}) = \text{zero}$. E_{s3} causes a current to flow only in R_{C2}; therefor , $i_3 = f(E_{s3}) = E_{s3})/(R_{C2})$.

By superposition,

$$i_s = i_1 + i_2 + i_3. \tag{21}$$

Also, by superposition, letting E_{s2} and E_{s3} be set equal to zero, i_1 becomes

$$i_1 = i_1(E_{s1}) + i_2(E_{s1}) + i_3(E_{s1}) \tag{22}$$

(zero)

this is $i_1(E_{s1})$

$$i_1 = \left[\frac{E_{s1}}{R_f + (R_{E1} \| R_i) \| \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]$$

this is $i_2(E_{s1})$

$$+ \left[\frac{E_{s1}}{R_f + (R_{E1} \| R_i) \| \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{(R_{E1} \| R_i)}{(R_{E1} \| R_i) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2). \tag{23}$$

Letting E_{s1} and E_{s3} be set equal to zero, $i_2 = f(E_{s2})$ becomes

$$i_2 = i_1(E_{s2}) + i_2(E_{s2}) + i_3(E_{s2}) = \text{zero} + \text{zero} + \text{zero}. \tag{24}$$

Letting E_{s1} and E_{s2} be set equal to zero, $i_3 = f(E_{s3})$ becomes

$$i_3 = i_1(E_{s3}) + i_2(E_{s3}) + i_3(E_{s3}) \tag{25}$$

$$i_3 = \text{zero} + \text{zero} + \frac{E_{s3}}{R_{C2}}. \tag{26}$$

Combining the results by superposition and letting $(E_{s1} = E_{s2} = E_{s3}) = E_s$, $I_s = (i_1 + i_2 + i_3)$ becomes

$$I_x = \left[\frac{E_{x1}}{R_f + (R_{E1}\|R_i)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left\{1 + \left[\frac{(R_{E1}\|R_i)}{(R_{E1}\|R_i) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)\right\} + \left[\frac{E_{x2}}{R_{C2}}\right]. \quad (27)$$

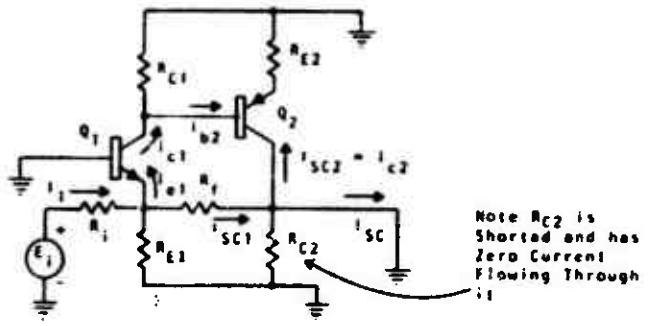


Fig. 11. Circuit diagram for short circuit calculations.

Therefore, DPI_{out} is, by interpreting (27) to represent current in parallel impedances,

$$DPI_{out} = \left\{\frac{\left[R_f + (R_{E1}\|R_i)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]\right]}{1 + \left[\frac{(R_{E1}\|R_i)}{(R_{E1}\|R_i) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)}\right\}\|(R_{C2}). \quad (28)$$

this is the factor that makes DPI_{out} small

The short-circuit output current I_{SC} due to E_i can be written out by superposition and inspection by referring to the circuit diagram shown in Fig. 11. With E_x = zero and the output shorted, the input current I_i can be written by inspection

$$I_i = \frac{E_i}{DPI} = \left[\frac{E_i}{R_i + (R_{E1})\|(R_f)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right] \quad (29)$$

and short-circuit current consists of the current through R_f and the collector current of Q_2; thus, I_{SC} becomes

$$I_{SC} = I_{SC1} - I_{SC2} \quad (30)$$

$$I_{SC} = I_i\left[\frac{(R_{E1})\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}{R_f + (R_{E1})\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right] - I_i\left[\frac{(R_{E1}\|R_f)}{(R_{E1}\|R_f) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\cdot\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2). \quad (31)$$

And since I_i is a common term, I_{SC} can be written as

$$I_{SC} = \left[\frac{E_i}{R_i + (R_{E1})\|(R_f)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left\{\left[\frac{(R_{E1})\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}{R_f + (R_{E1})\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right] - \left[\frac{(R_{E1}\|R_f)}{(R_{E1}\|R_f) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)\right\}. \quad (32)$$

The open-circuit (no-load) output voltage is $E_{out} = (I_{sc})(DPI_{out})$; therefore, combining I_{sc} from (32) and DPI_{out} from (28), the output voltage with feedback becomes

$$E_{out} = \overbrace{\left[\frac{E_i}{R_i + (R_{B1})\|(R_f)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]}^{I_i} \overbrace{\left\{\left[\frac{(R_{B1})\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}{R_f + (R_{B1})\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\right.}^{\text{direct feedthrough term}}$$

$$\overbrace{\left. - \left[\frac{(R_{B1}\|R_f)}{(R_{B1}\|R_f) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)\right\}}^{\text{main feedback term}}$$

$$\underbrace{\left\{\left[\frac{\left[R_f + (R_{B1}\|R_i)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]\right]}{1 + \left[\frac{(R_{B1}\|R_i)}{(R_{B1}\|R_i) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_1)R_{E1}}\right](\beta_2)}\right]\|(R_{C2})\right\}}_{\text{main } DPI_{out} \text{ term due to feedback}} . \tag{33}$$

Observing the relative magnitudes of the various terms of the E_{out} equation (by substituting numerical values), one soon recognizes that the negative main feedback term predominates over the positive direct feedthrough term and thus the direct feedthrough term can be often neglected. Also, one notices that the main DPI_{out} term due to feedback is much smaller than R_{C2} with which it is paralleled and thus predominates so that R_{C2} in the DPI_{out} expression can be neglected. Neglecting these terms leaves us with the following approximate answer for E_{out}:

$$E_{out} \cong \underbrace{\left[\frac{E_i}{R_i + (R_{B1})\|(R_f)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]}_{\text{approaches } [E_i/R_i]} \left\{ \overbrace{- \left[\frac{(R_{B1}\|R_f)}{(R_{B1}\|R_f) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]}^{\text{approaches unity since } (R_{B1}\|R_f) \gg [(h_{ie1})/(1+\beta_1)]} \left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie1} + (1+\beta_2)R_{E2}}\right](\beta_2) \right\}$$

$$\left\{ \frac{\overbrace{\left[R_f + (R_{B1}\|R_i)\|\left[\frac{h_{ie1}}{1+\beta_1}\right]\right]}^{\text{approaches } R_f}}{\left[\frac{(R_{B1}\|R_i)}{(R_{B1}\|R_i) + \left[\frac{h_{ie1}}{1+\beta_1}\right]}\right]\left[\frac{\beta_1}{1+\beta_1}\right]\left[\frac{R_{C1}}{R_{C1} + h_{ie2} + (1+\beta_2)R_{E2}}\right](\beta_2)} \right\} . \tag{34}$$

cancels with terms below

cancels with terms above

approaches unity since $(R_{B1}\|R_i) \gg [(h_{ie1})/(1+\beta_1)]$

The expression for E_{out} can be further simplified by cancelling identical numerator and denominator terms, noting that two current-divider expressions are approximately unity and observing that a numerator term approaches R_f and a denominator term approaches R_i, respectively, because $R_f \gg (R_{B1})\|(R_i)\|[(h_{ie1})/(1+\beta_1)]$ and $R_i \gg (R_{B1})\|(R_f)\|[(h_{ie1})/(1+\beta_1)]$. The more simplified expression for E_{out} is

$$E_{out} \cong -E_i \frac{R_f}{R_i} \tag{35}$$

and is the expression given in most other publications (without proof).

This paper would not be complete if part of the two-

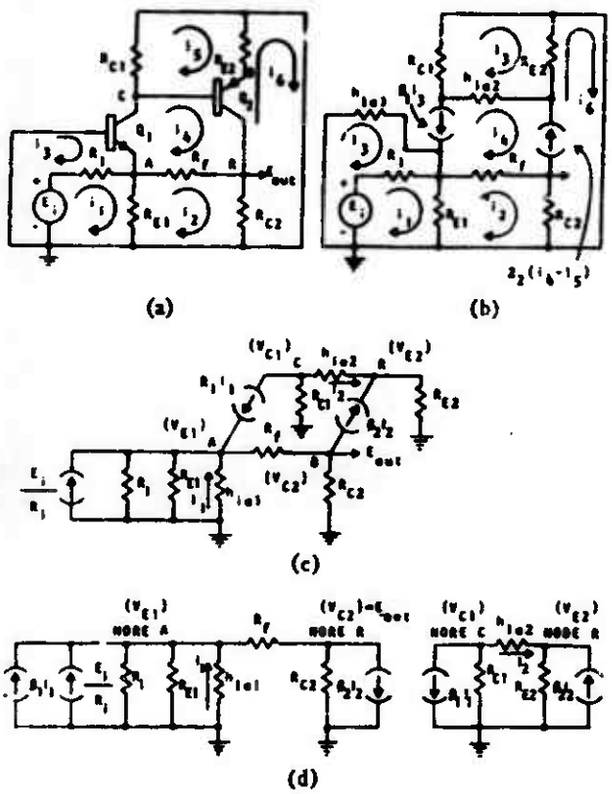


Fig. 12. Circuit diagrams for loop and node analysis of feedback amplifier.

stage feedback amplifier were not analyzed by some conventional method such as loop or node analysis. In Fig. 12(a) and 12(b) the signal circuit diagram is redrawn for possible loop analysis. Although there are six loops shown, closer inspection will reveal that the i_1 and i_3 loops can be easily eliminated by Thevenin's theorem so that only a four-loop set of equations must be solved. Since it is desired to solve for E_{out}, it is more appropriate to use node analysis and solve for the single voltage V_{C2}.

The circuit is redrawn in Fig. 12(c) for nodal analysis. In Fig. 12(d), the nodal-analysis circuit diagram is further simplified by drawing each node-to-node current source as two individual current sources between each respective node and common ground. Referring to Fig. 12(d), the set of node equations are expressed in general terms in (36)–(39). The node analysis is as follows.

Node A:

$$\sum I_{AA} = + V_A\left[\frac{1}{R_{AA}}\right] - V_B\left[\frac{1}{R_{AB}}\right] - V_C\left[\frac{1}{R_{AC}}\right] - V_D\left[\frac{1}{R_{AD}}\right]. \quad (36)$$

Node B:

$$\sum I_{BB} = - V_A\left[\frac{1}{R_{BA}}\right] + V_B\left[\frac{1}{R_{BB}}\right] - V_C\left[\frac{1}{R_{BC}}\right] - V_D\left[\frac{1}{R_{BD}}\right]. \quad (37)$$

Node C:

$$\sum I_{CC} = - V_A\left[\frac{1}{R_{CA}}\right] - V_B\left[\frac{1}{R_{CB}}\right] + V_C\left[\frac{1}{R_{CC}}\right] - V_D\left[\frac{1}{R_{CD}}\right]. \quad (38)$$

Node D:

$$\sum I_{DD} = - V_A\left[\frac{1}{R_{DA}}\right] - V_B\left[\frac{1}{R_{DB}}\right] - V_C\left[\frac{1}{R_{DC}}\right] + V_D\left[\frac{1}{R_{DD}}\right]. \quad (39)$$

The appropriate values pertinent to Fig. 12(d) are substituted and the results given in (40)–(43). Because the circuit is that of a feedback amplifier with two dependent current sources, two additional equations are required to describe these dependent sources. The ones describing I_1 and I_2 are (44) and (45), respectively.

Node A:

$$\left[\beta_1 I_1 + \frac{E_i}{R_i}\right] = + V_{E1}\left[\frac{1}{R_i \| R_{E1} \| h_{ie1} \| R_f}\right] - V_{C2}\left[\frac{1}{R_f}\right] - [\text{zero}] - [\text{zero}]. \quad (40)$$

Node B:

$$[-\beta_2 I_2] = - V_{E1}\left[\frac{1}{R_f}\right] + V_{C2}\left[\frac{1}{R_f \| R_{C2}}\right] - [\text{zero}] - [\text{zero}]. \quad (41)$$

Node C:

$$[-\beta_1 I_1] = - [\text{zero}] - [\text{zero}] + V_{C1}\left[\frac{1}{R_{C1} \| h_{ie2}}\right] - V_{E2}\left[\frac{1}{h_{ie2}}\right]. \quad (42)$$

Node D:

$$[+\beta_1 I_2] = - [\text{zero}] - [\text{zero}] - V_{C1}\left[\frac{1}{h_{ie2}}\right] + V_{E2}\left[\frac{1}{h_{ie2} \| R_{E2}}\right]. \quad (43)$$

$$I_1 = \left[-\frac{V_{E1}}{h_{ie1}}\right]. \quad (44)$$

$$I_2 = \left[\frac{V_{C1} - V_{E2}}{h_{ie2}}\right]. \quad (45)$$

Substituting (44) and (45) into (41)–(43), we obtain the final set of node equations, (46)–(49). This final set of node equations can be solved by standard techniques for any of the node voltages.

Node A:

$$\left[\frac{E_i}{R_i}\right] = + V_{E1}\left[\frac{1}{R_i \| R_{E1} \| \left[\frac{h_{ie1}}{1+\beta_1}\right] \| R_f}\right]$$

$$- V_{C2}\left[\frac{1}{R_f}\right] - V_{C1}[\text{zero}] - V_{E2}[\text{zero}]. \quad (46)$$

Node B:

$$0 = - V_{E1}\left[\frac{1}{R_f}\right] + V_{C2}\left[\frac{1}{R_f \| R_{C2}}\right] + V_{C1}\left[\frac{1}{\left[\frac{h_{ie2}}{\beta_2}\right]}\right] - V_{E2}\left[\frac{1}{\left[\frac{h_{ie2}}{\beta_2}\right]}\right] \quad (47)$$

Node C:

$$0 = - V_{E1}\left[\frac{1}{\left[\frac{h_{ie1}}{\beta_1}\right]}\right] - V_{C2}[\text{zero}] + V_{C1}\left[\frac{1}{R_{C1} \| h_{ie2}}\right] - V_{E2}\left[\frac{1}{h_{ie2}}\right] \quad (48)$$

Node D:

$$0 = - V_{E1}[\text{zero}] - V_{C2}[\text{zero}] - V_{C1}\left[\frac{1}{\left[\frac{h_{ie2}}{1+\beta_2}\right]}\right] + V_{E2}\left[\frac{1}{R_{E2} \| \left[\frac{h_{ie2}}{1+\beta_2}\right]}\right] \quad (49)$$

Equation (50) is the solution for $V_{C2} = E_{out}$ expressed as the ratio of two determinates. Equation (50) can be evaluated by minors and will have four terms in the numerator and six terms in the denominator. The expansion of the ratio of determinates results in an answer for E_{out} which is not easy for an average person to interpret. Obtaining the answer for E_{out} in the form given by (50) involved a lengthy process and the result did not readily reveal a great insight into circuit action, and, in addition, it provided only one of the three answers asked for in the problem. DPI_{in} and DPI_{out} must be calculated using other techniques and each answer will be of the same form as (50) if standard loop and node analysis methods are employed.

$$V_{C2} = E_{out} = \frac{\begin{vmatrix} \left[\frac{1}{R_i \| R_{E1} \| \left[\frac{h_{ie1}}{1+\beta_1}\right] \| R_f}\right] & \left[\frac{E_i}{R_i}\right] & 0 & 0 \\ -\left[\frac{1}{R_f}\right] & 0 & \left[\frac{1}{\left[\frac{h_{ie2}}{\beta_2}\right]}\right] & -\left[\frac{1}{\left[\frac{h_{ie2}}{\beta_2}\right]}\right] \\ -\left[\frac{1}{\left[\frac{h_{ie1}}{\beta_1}\right]}\right] & 0 & \left[\frac{1}{R_{C1} \| h_{ie2}}\right] & -\left[\frac{1}{h_{ie2}}\right] \\ 0 & 0 & -\left[\frac{1}{\left[\frac{h_{ie2}}{1+\beta_2}\right]}\right] & \left[\frac{1}{R_{E2} \| \left[\frac{h_{ie2}}{1+\beta_2}\right]}\right] \end{vmatrix}}{\begin{vmatrix} \left[\frac{1}{R_i \| R_{E1} \| \left[\frac{h_{ie1}}{1+\beta_1}\right] \| R_f}\right] & -\left[\frac{1}{R_f}\right] & 0 & 0 \\ -\left[\frac{1}{R_f}\right] & \left[\frac{1}{R_f \| R_{C2}}\right] & \left[\frac{1}{\left[\frac{h_{ie2}}{\beta_2}\right]}\right] & -\left[\frac{1}{\left[\frac{h_{ie2}}{\beta_2}\right]}\right] \\ -\left[\frac{1}{\left[\frac{h_{ie1}}{\beta_1}\right]}\right] & 0 & \left[\frac{1}{R_{C1} \| h_{ie2}}\right] & -\left[\frac{1}{h_{ie2}}\right] \\ 0 & 0 & -\left[\frac{1}{\left[\frac{h_{ie2}}{1+\beta_2}\right]}\right] & \left[\frac{1}{R_{E2} \left[\frac{h_{ie2}}{1+\beta_2}\right]}\right] \end{vmatrix}} \quad (50)$$

Conclusion

The DPI analysis technique set forth in this paper provides a method for rapidly analyzing electronic circuits. It is applicable to ordinary circuits as well as those that involve feedback. The most important advantage of the DPI analysis technique is that the answers, written out by inspection, are in the form of simple Ohm's law equations involving the current-divider equation and the voltage-divider equation. Any voltage, any current, or any driving point impedance can be written out with equal ease.

Although no examples were given in this paper, the techniques are equally applicable to determining dc operating conditions and even the effects of base-emitter offset voltages can be taken into consideration in the dc calculations by taking into account their contribution to the superposition sum. Since the methods apply to dc calculations, the complete analysis of such feedback circuits as regulated power supplies can be readily performed.

Because of the simplicity of form exhibited by the answers, even inexperienced people rapidly gain a feel for the electronic circuit. When a person gains a feel for the circuit he is an electroniker.

APPENDIX D

TABLES OF TRANSISTOR AND DIODE EMP PARAMETERS

The following tables are a listing of measured and calculated damage constants and other pertinent data for diodes and transistors. This listing is a compilation of data acquired during various EMP programs and is provided as an aid to further studies.

NOTES:

1. For SCR's, Breakdown taken Anode to Cathode.
2. Reference Source data:
   a. SP - SAP-1 Computer Listing
   b. DX - Experimental data from DASA Handbook
   c. DE - Estimated data from DASA Handbook
   d. CM - Computed data
3. * indicates a unijunction device - the value under BV_{EBO} is V_{B1E} and the value under BV_{CBO} is V_{B1B2}.
4. -- indicates the column is not pertinent to the device; a blank indicates the information is not available.
5. † indicates a FET device - the value under BV_{EBO} is BV_{dss}, and the value under BV_{CBO} is BV_{gss}.
6. Parameter Definitions:

   BV_{CBO} - Collector to Base breakdown voltage with the Emitter open

   BV_{CEO} - Collector to Emitter breakdown voltage with the Base open

   V_{B1E} - Emitter to Base 1 voltage

   V_{B1B2} - Base 1 to Base 2 voltage

   BV_{dss} - Drain to Source breakdown voltage with the Gate shorted

   BV_{gss} - Gate to Source breakdown voltage with the Drain shorted

TABLE D-1

DIODE EMP DATA

Device Number	K	V_{BD}	Reference
IN23B, C	.0009		SP
IN23RF	.00094		DX
IN23WE	.00029		DX
IN25	.026		DX
IN34A	.014	60.	DX
IN39A	.006	230.	SP
IN39B	.006	200.	SP
IN43B	.005	70.	CM
IN64	.041	25.	DX
IN67A	.003	80.	SP
IN69, A	.005	70.	CM
IN81	.003	10.	SP
IN82A	.0007	5.	DX
IN91	.0055	100.	CM
IN128	.005	40.	CM
IN191	.005	90.	SP
IN198	.024	80.	SP
IN248A	40.	50.	SP
IN249	40.	100.	SP
IN249B	40.	100.	SP
IN250	40.	200.	SP
IN250B	80.	200.	SP, DE
IN251	.03	40.	SP
IN253	86.	95.	DX
IN254	3.5	190.	SP
IN260	.0027	30.	CM
IN270	.022	100.	CM
IN276	.0055	100.	CM
IN277	.027	125.	DX

TABLE D-1

DIODE EMP DATA

Device Number	K	V_{BD}	Reference
IN295, A	.005	40.	SP
IN320	1.2	500.	SP
IN332	3.5	400.	SP
IN333	1.5	400.	SP
IN335	1.5	300.	SP
IN337	1.5	200.	SP"
IN338	18.3	100.	DE
IN341	3.5	400.	SP
IN342	1.5	400.	SP
IN346	1.5	200.	SP
IN429	.6	6.2	DX
IN457	.12	70.	DX
IN458	.5	150.	SP
IN459	.59	200.	DX
IN459A	.96	200.	DX
IN461	.24	35.	SP
IN462	.05	80.	SP
IN466	.78	3.5	SP
IN467	.78	4.1	SP
IN468	.78	4.9	SP
IN470	.78	7.1	SP
IN474A	.219	5.8	CH
IN482A	.96	36.	DX
IN483, A	.3	70.	SP
IN483, B	.3	^ 80.	SP
IN484A	.45	130.	DX
IN484B	.3	130.	SP
IN485	.3	180.	CH
IN486, B	.29	225.	SP

TABLE D-1

DIODE EMP DATA

Device Number	K	V_{BD}	Reference
IN487, Z	.3	300.	SP
IN488	.3	380.	SP
IN536	1.	50.	DE
IN537	.51	100.	DX
IN538, M	1.	200.	SP
IN539	1.	300.	SP
IN540	.93	400.	OX
IN547	12.1	600.	DX
IN560	.625	800.	CM
IN561	.625	1000.	CM
IN562	1.8	800.	SP
IN619	.36	10.	SP
IN622	.347	150.	CM
IN625	.164	30.	CM
IN625A	.045	20	CM
IN643	.44	200.	SP
IN643A	.1	200.	DX
IN645	2.8	225.	SP
IN646	2.29	300.	DX
IN647	2.8	400.	SP
IN648	2.8	500.	SP
IN649	2.9	600.	DX
IN658	.92	120	OX
IN660	.44	100.	SP
IN661	.41	200.	DX
IN662	.29	100.	SP
IN663	.44	100.	SP
IN676	.27	100.	SP
IN689	1.1	600.	SP

TABLE D-1
DIODE EMP DATA (Continued)

Device Number	K	V_{BD}	Reference
IN691	.418	80.	SP
IN692	.5	100.	SP
IN702, A	1.	2.6	SP, DX
IN703A	1.	3.5	SP
IN704, A	1.	4.1	SP
IN705, A	.91	4.8	SP
IN706	.288	5.8	CM
IN709, A	.78	6.2	SP
IN710	.78	6.8	SP
IN711A	2.1	7.5	DX
IN712	.78	8.2	SP
IN714A	.78	10.	SP
IN715A	.78	11.	SP
IN718A	.1	15.	SP
IN719A	.1	16.	SP
IN721, A	.35	20.	SP
IN725A	.349	30.	CM
IN729	.06	43.	SP
IN746, A	1.1	3.3	SP
IN747, A	1.1	3.6	SP
IN748A	1.1	3.9	SP
IN749	1.1	4.3	SP
IN750A	1.1	4.7	SP
IN751, A	1.1	5.1	SP
IN752, A	1.1	5.6	SP
IN753, A	1.2	6.2	SP, DX
IN754, A	.63	6.8	SP
IN755, A	.63	7.5	SP
IN756, A	.63	8.2	SP

TABLE D-1

DIODE EMP DATA (Continued)

Device Number	K	V_{BD}	Reference
IN757, A	.63	9.1	SP
IN758, A	.63	10.	SP
IN759, A	.63	12.	SP
IN761	1.8	4.9	SP
IN762	1.8	5.8	SP
IN763	1.8	7.1	SP
IN763-2	3.	7.0	DX
IN766A	1.8	12.8	SP
IN767	1.8	15.8	SP
IN769A	1.8	23.5	SP
IN769-3	2.	26.	DX
IN816, W	1.5	26.	DX
IN817	.46	200.	SP
IN821	.577	6.2	CM
IN823	1.8	6.2	DX
IN845	.365	200.	CM
IN890	.357	60.	CM
IN914	.85	100.	DX
IN916	.44	100.	SP
IN933	.014	100.	DX
IN933J	.1	100.	DX
IN936	.14	9.	DX
IN936A, B	7.	9.	SP
IN937	.824	9.	CM
IN938A, B	7.	9.	SP
IN939	.824	9.	CM
IN939B	7.0	9.	DE
IN960B	1.0	9.	SP
IN961B	1.0	10.	SP
IN963B	1.	12.	SP

TABLE 0-1

DIODE EMP DATA (Continued)

Device Number	K	V_{BD}	Reference
IN964B	1.	13.	SP
IN965B	1.	15	SP
IN967B	.73	18.	OX
IN968B	1.	20.	SP
IN969B	1.	22.	SP
IN970B	1.	24.	SP
IN972B	1.	30.	SP
IN973B	1.	33.	SP
IN974B	1.	36.	SP
IN975B	1.	39.	SP
IN976B	1.	43.	SP
IN977B	1.	47.	SP
IN979B	1.	56.	SP
IN981B	1.4	68	OX
IN983A	1.	82.	SP
IN987A, B	1.	120.	SP
IN1095	.9	500.	DX
IN1096	.9	600.	SP
IN1118	11.392	400.	CM
IN1124A	7.985	250.	CM
IN1126A	14.	500.	SP
IN1184	31.5	100.	CM
IN1199, A	15.	50.	SP
IN1200	62.32	100.	CM
IN1201	62.32	150.	CM
IN1202	21.	200.	SP
IN1204A	46.106	400.	CM
IN1206	62.32	600.	CM
IN1217	5.8		SP
IN1222B	2.563	400.	CM

TABLE 0-1
0100E EMP 0ATA (Continued)

Oevice Number	K	V_{BO}	Reference
IN1317A	.19	19.	SP
IN1319A	.19	28.	SP
IN1342A	38.4	100.	DE
IN1348A	1.827	200.	CM
IN1367	34.	47.	SP
IN1583	11.391	200.	CM
IN1585	3.5	400.	DE
IN1614	.38	200.	SP
IN1615	.666	480.	CM
IN1693	3.2	200.	SP
IN1695	3.2	400.	SP
IN1731	3.2	1500.	CM
IN1733A	11.3	3000.	DE
IN1770A	14.2	9.1	DE
IN1773A	1.9	12.	SP
IN1780A	1.9	24.	SP
IN1783	21.3	33.	DE
IN1818RA	4.3	16.	SP
IN1823C, A	4.3	27.	SP
IN1828C	4.3	43.	SP
IN1834	33.8	75.	CM
IN1835A	4.3	82.	SP
IN1836C	4.3	91.	SP
IN1904	28.	100.	SP
IN1909	6.8	200.	SP
IN2037	.05	12.8	SP
IN2154	20.	50.	SP
IN2158	21.5	400.	CM
IN2164	2.3	9.4	SP
IN2483	2.1	400.	SP

TABLE D-1

DIODE EMP DATA (Continued)

Device Number	K	V_{BD}	Reference
IN2610	2.6	100.	SP
IN2611	2.6	200.	SP
IN2613	2.6	400.	SP
IN2615	2.6	600.	SP
IN2,89	40.	400.	SP
IN2795	40.	150.	SP
IN2796	40.	200.	SP
IN2808	249.	10.	CM
IN2818	249.	20.	CM
IN2823B	249.	30.	CM
IN2824	156.	33.	SP
IN2826B	249.	39.	CM
IN2844B	15.	160.	SP
IN2846B	15.	200.	SP
IN2862	2.8	400.	SP
IN2864	2.8	600.	SP
IN2929A	.073	1.	DX
IN2930	.196	.74	CM
IN2970B	15.0	6.8	SP
IN2976B	15.	12.	SP
IN2979B	15.	15.	SP
IN2984, B	15.	20.	SP
IN2985, B, RB	15.	22.	SP
IN2986B	15.	24.	SP
IN2987B	15.	25.	SP
IN2988B	15.	27	SP
IN2989B	15.	30.	SP
IN2991B	15.	36.	SP
IN2995, B	15.	47.	SP
IN2997B	15.	51.	SP

TABLE D-1

DIODE EMP DATA (Continued)

Device Number	K	V_{BD}	Reference
1N3001B	15.	68.	SP
1N3008B	15.	120.	SP
1N3015B	33.84	200.	CM
OM3-;6B	19.5	6.8	DE
1N3017B	1.9	7.5	SP
1N3019B	1.9	9.1	SP
1N3022B	1.9	12.	SP
1N3024B	1.9	15.	SP
1N3025B	1.9	16.	SP
1N3026B	1.9	18.	SP
1N3027B	1.9	20.	SP
1N3028, B	1.9	22.	SP
1N3029B	1.9	24.	SP
1N3030B	1.9	27.	SP
1N3031B	1.9	30.	SP
1N3033B	1.9	36.	SP
1N3035B	1.9	43.	SP
1N3037B	1.9	51.	SP
1N3040B	1.9	68.	SP
1N3041, B	1.9	75.	SP
1N3051B	1.9	200.	SP
1N3064	.02	75.	SP
1N3070	.365	200.	CM
1N3157	.625	8.4	CM
1N3189	10.	200.	SP
1N3190	4.1	600.	CM
1N3560	.038	.475	CM
1N3561	.038	.475	CM
1N3582A	.35	11.7	SP

TABLE D-1

DIODE EMP DATA (Concluded)

Device Number	K	V_{BD}	Reference
1N3600	.18	50.	SP
1N3821	1.947	3.3	CM
1N3828A	1.95	6.2	CM
1N3893	6.41	400.	CM
1N3976	132.	200.	CM
1N4241	33.84	6.	CM
1N4245	2.4	200.	SP
1N4249	2.4	1000.	SP
1N4312	.116	150.	CM
1N4370A	.625	2.4	CM
1N4816	6.8	50	DE
1N4817	6.8	100.	DE
1N4820	10.	400.	DE
1N4823	.208	100V	CM
1N4989	14.33	200.	CM
AM2	1.4	50.	SP
D4330	.001		SP
FD300	.18	125.	SP
SG22	.23		SP
SL010EC		10,000.	CM
SV1035	1.71	26.	CM
SV2092	2.6		SP
SV2183	2.6		SP
TM7	20.	70.	SP
TM21	18.	200.	SP
TM27	20.	200.	SP
TM84	11.	800.	SP
TM124	11.	1200.	SP
UT 242	2.6	200.	SP

TABLE D-2

TRANSISTOR EMP DATA

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N43,A	.28	5.	45.	30.	SP
2N117	.15	1.	45.	45.	SP
2N118	.15	1.	45.	45.	SP
2N128	.017	10.	10.	4.5	SP
2N158	.499	30.	60.	60.	CM
2N176	.46		40.	30	CM
2N189	.17		25.	25.	SP
2N190	.58		25.	25.	DX
2N243	.05	1.	60.	60.	SP
2N244	.05	1.	60.	60.	SP
2N263	.38	1.	45.	30.	SP
2N264	.36		45.	30.	SP
2N274	.0076	.5	35.	40.	CM
2N279A	.047		45.	30	CM
2N297A	.499	40.	60.	40.	CM
2N329,A	.21	20.	50.	30.	SP
2N332	.45	1.	45.	30.	SP
2N333	.32	1.	45.	30.	SP
2N335,A	.55	1. (4.-2N335A)	45	45.	SP
2N336	.55	1.	45.	30.	SP
2N337	.12	1.	45.	30.	SP
2N338	.12	1.	45.	30.	SP
2N339	2.	1.	55.	55.	SP
2N341	1.	1.	125.	85.	SP
2N343	.047	1.	60.	60.	SP, DX
2N343A	.05	1.	60.	60.	SP
2N357	.05	20.	20.	15.	SP
2N359	.04	6.	25.	18.	SP

TABLE D-2

TRANSISTOR EMP DATA (Continued)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N375	1.02	40.	80.	60.	OX
2N388	.084	15.	25.	20.	CM
2N389	2.14	10.		60.	OX
2N395	.09	20.	30.	15.	SP
2N404	.05	12.	25	24.	CM
2N424A	10.	10.	80.	80.	SP
2N463	6.6	50.	60.	60.	DX
2N480	.132	2.	45.	45.	CM
2N490	1.	60.*	58.*	--	SP
2N491	1.	60.*	58.*	--	SP
2N495,A	.7	20.	25.	25.	SP
2N497	.8	8.	60.	60.	SP
2N498	.8	8.	100.	100.	DX
2N525	.3	15.	45.	30.	SP
2N526	.39	15.	45.	30.	DX
2N527	.3	15.	45.	30.	SP
2N537	.012	1.	30.		CM
2N538	.5285	28.	80.	60	CM
2N539.A	6.	28.	80.	55.	SP
2N540	.5285	28.	80.	55.	CM
2N542	.18	2.	30.	30.	SP
2N551	1.6	6.	60.	60.	SP
2N576A	.023	15.	40.	20.	DX
2N587	.14	40.	40.	30.	SP
2N595	.012		20.	15.	CM
2N618	.88	40.	80.	60.	DX
2N652A	.118	30.	45.	30.	CM
2N656	.2	8.	60.	60.	OX
2N657	.66	8.	100.	100.	OX

TABLE D-2

TRANSISTOR EMP DATA (Continued)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N657A	1.07	8.	100.	100.	DX
2N682	.33	--	--	50. (A-C)	CM
2N685	1.4	--	--	200. (A-C)	DX
2N687	11.7	--	--	300. (A-C)	DX
2N690	3.1	--	--	800. (A-C)	CM
2N696	1.0	5.	60.	40.	CM
2N697	.2	5.	60.	40.	SP
2N699	.25	5.	120.	80.	DX
2N703	.08	5.	25.	25.	SP
2N706,8	.0075	3. (5.-2N706B)	25.	20.	DX
2N708	.03	5.	40.	15.	DX
2N717	.13	5.	60.	40.	SP
2N718	.13	5.	60.	40.	SP
2N718A	.35	7.	75.	32.	SP
2N726	.021	5.	25.	20.	CM
2N730	.165	5.	60.	40.	CM
2N736	.1	5.	80.	60.	DX
2N756A	.32	6.	60.	60.	SP
2N757	.032	6.	45.	45.	CM
2N760A	.034	8.	60.	60.	DX
2N834	.03	5.	40.	30.	SP
2N859	.18	25.	40.	40.	DX
2N869A	.009	5.	25.	18.	CM
2N910	.218	7.	100.	60.	CM
2N912	.07	7.	100.	60.	SP
2N914	.04	5.	40.	15.	SP
2N916	.043	5.	45.	25.	CM
2N917	.004	3.	30.	15.	SP

TABLE D-2

TRANSISTOR EMP DATA (Continued)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N918	.004	3.	30.	15.	CM
2N927	.1	70.	70.	60.	OX
2N930	.046	5.	45.	45.	OX
2N930A	.02	6.	60.	45.	DX
2N1016,B	1.6	25.	100.	100.	DX
2N1039	1.4	20.	60.	60.	DX
2N1045-1	.55	20.	100.	60.	SP
2N1048	3.9	6.	120.	120.	SP
2N1049	3.9	6.	80.	80.	SP
2N1050	6.082	6.	120.	120.	CM
2N1069	9.3	9.	60.	45.	SP
2N1099	1.	40.	80.	60.	OX
2N1115	.38		20.	15.	DX
2N1116A	.98	6.	60.	60.	DX
2N1118	.19	10.	25.	25.	OX
2N1132	.23	5.	50.	35.	DX
2N1136B	18.4		100.	65.	SP
2N1150	.18	1.	45.		SP
2N1154	21.	1.	50.	28.	SP
2N1156	18.	1.	120.	68.	SP
2N1184	.471	20.	45.	20.	CM
2N1212	13.129	10.	60.	60.	CM
2N1303	.087	25.	30.		CM
2N1308	.084	25.	25.	15.	CM
2N1309	.087	25.	30.		CM
2N1445	.5	8.	120.	120.	SP
2N1458	.5285	15.	80.	65.	CM
2N1469	.65	40.	40.	35.	DX
2N1480	5.5	12.	100.	55.	SP

TABLE D-2

TRANSISTOR EMP DATA (Continued)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N1481	2.2	12.	60.	40.	SP
2N1483	3.633	12.	60.	40.	CM
2N1485	4.1	12.	60.	40.	SP
2N1486	5.	12.	100.	55.	SP
2N1489	12.3	10.	60.	40.	SP
2N1490	12.3	10.	100.	55.	SP
2N1564	.56	5.	80.	60.	SP
2N1565	.11	5.	80.	60.	SP
2N1566	.11	5.	80.	60.	SP
2N1596	.94	--	--	100.	DX
2N1602	.40	--	--	200.	DX
2N1613	.27	7.	75.	50.	SP
2N1615	.553	8.	100.	100.	CM
2N1642	.13	30.	30.	6.	DX
2N1700	4.134	6.	60.	40.	CM
2N1701	4.5	6.	60.	40.	SP
2N1711	.36	7.	75.	50.	SP
2N1722	54.5	10.	175.	80.	DX
2N1751	1.05	2.5	80.	80.	CM
2N1753	.039	.5	30.	18.	CM
2N1772A	.651	--	--	100.	CM
2N1776A	1.584	--	--	300.	CM
2N1777A	C-G C-A 2.0 .46	--	--	400.	DX
2N1871A	1.1	--	--	60.	CM
2N1890	.27	7.	100.	60.	SP
2N1893	.4	7.	120.	80.	DX
2N1916W	2.22	--	--	400.	CM
2N2015	26.462	10.	100.	50.	CM
2N2035	3.633	10.	80.	60.	CM

TABLE D-2

TRANSISTOR EMP DATA (Continued)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N2060	.21	7.	100.	60.	SP
2N2102	.77	7.	120.	65.	SP
2N2156	.471	25.	45.	30.	CM
2N2218A	.264	6.	75.	40.	CM
2N2219	.3	5.	60.	30.	SP
2N2219A	.264	6	75.	40.	CM
2N2222	.1	5.	60.	30.	DX
2N2222A	.1	6.	75.	40.	SP
2N2223,A	.21	7.	100.	60.	SP
2N2270	.5	7.	60.	45.	SP
2N2346	3.2	--	--	100.	DX
2N2369A	.03	4.5	40.	15.	SP
2N2417	.549	30.*	35.*	--	CM
2N2432	.189	15.	30.	30.	CM
2N2481	.099	5.	40.	15.	CM
2N2509	.126	7.	125.	80.	CM
2N2516	.209	8.	80.	60.	CM
2N2563	.55	20.	100.	100.	SP
2N2646	.72	30.*	35.*	--	SP
2N2708	.018	3.	35.	20.	CM
2N2857	.018	2.5	30.	15.	CM
2N2894,A	.03	4. (4.5-2N2894A)	12.	12.	SP
2N2904A	.221	5.	60.	60.	CM
2N2905	.221	5.	60.	40.	CM
2N2906	.044	5.	60.	40.	DX
2N2906A	.221	5.	60.	60.	CM
2N2907,A	.1	5.	60.	40. (60.-A)	DX
2N2920	.04	6.	60.	60.	DX

TABLE D-2

TRANSISTOR EMP DATA (Continued)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
2N2996	.01	.3	15.	10.	SP
2N3014	.02	5.	40.	20.	CM
2N3050	.01	5.	25.	20.	CM
2N3053	.721	5.	60.	40.	CM
2N3054	3.633	7.	90.	60.	CM
2N3055	20.084	7.	100.	70.	CM
2N3118	.53	4.	85.	60.	SP
2N3217	.126	15.	15.	10.	CM
2N3235	20.	7.	65.	55.	SP
2N3240	1.5	8.	160.	160.	SP
2N3251	.143	5.	50.	40.	CM
2N3308	.12	3.	30.	25.	SP
2N3384	.094	--	30.†	--	CM
2N3436	.488	--	50.†	--	CM
2N3440	1.75	7.	300.	250.	SP
2N3585	5.278	6.	440.	300	CM
2N3708	.507	6.	30.	30.	CM
2N3777	2.	8.	100.	100.	SP
2N3785	.012	.5	50.	12.	SP
2N3819	.22	25.†	25.†	--	CM
2N3823	.228	30.†	30.†	--	CM
2N3902	43.35	5.	400.	400.	CM
2N3907	.165	6.	60.	45.	CM
2N4037	.045	7.	60.	40.	CM

TABLE D-2

TRANSISTOR EMP DATA (Concluded)

Device Number	K	BV_{EBO}	BV_{CBO}	BV_{CEO}	Reference Source
LN75497	1.9				DX
LN75638	2.3				DX
MIS17331	.1				DX
T1482	.21	5.	20.	20.	SP
T1487	4.5	6.	80.	60.	SP
TIXM101	.01	.3	15.	7.	SP
SW3042	.1	--	--		DX

APPENDIX E

GENERALIZED EQUIVALENT CIRCUITS

1. THEORY

To make the cable analysis results readily applicable to subsystem assessment, it is often desirable to use a "Single Wire Equivalent Source" and "Black Box Driving Function." This is especially applicable for sub-circuit designers who do not have ready access to large scale computers and analysis codes. Figure E-1 illustrates the equivalent circuit of a typical cable/circuit interface. Looking to the left at terminals b-b, the source/line system has a Thevenin equivalent circuit in which $Z_g(f)$ is the frequency dependent impedance looking into terminals a-a when terminals b-b are open circuited and V is the open circuit voltage.

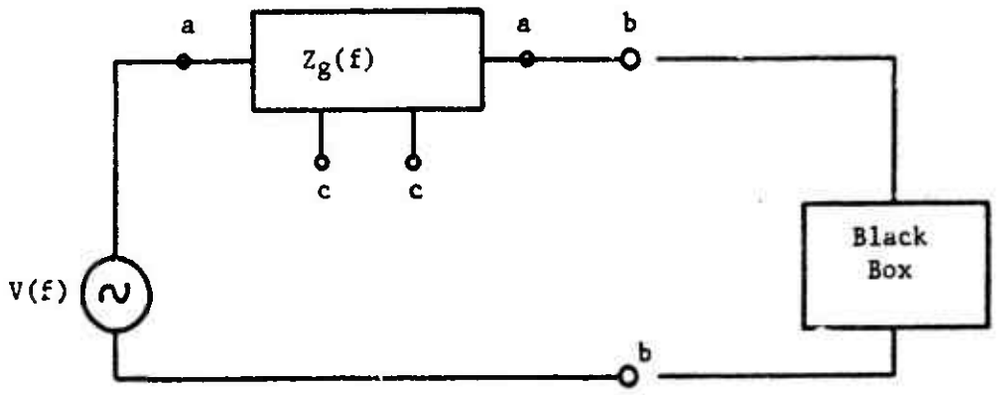


Figure E-1. Equivalent Circuit of Cable/Circuit Interface

In general, the circuit to the left of b-b may be represented by a simple Thevenin circuit, the "Single Wire Equivalent Source". Where now Z_g (f) repreaenta all other mutual or terminal Z's (such as direct connections to c-c, inductive and capacitive couplinga to other pairs, shield to pair coupling, cracks in shielding, etc.) V = V(f) is the total open circuit signal at b-b and may be a quite complicated function of frequency. Here the load elements to the right of b-b have been incorporated in a "black box" which represents the general circuit or component of ultimate interest. The "Black Box" as shown (a closed system) may contain active and passive devices and other sources, steady state or transient. How these are treated depends upon the ultimate analysis objective. At this level the problem has been treated as separable, i.e., the sources of EMP into b-b have been represented by $Z_g(f)$ and V_{oc}= V(f) which make up the "Black Box Driving Function."

$Z_g(f)$ might be estimated by analysis or measured. V_{oc} might be estimated by analysis, measured, or postulated; the latter is often the case. If postulated, it can be done in two forms: the frequency and the time domains. If postulated as a current waveform, then the Thevenin Equivalent goes over to a Norton Equivalent as shown in Figure E-2.

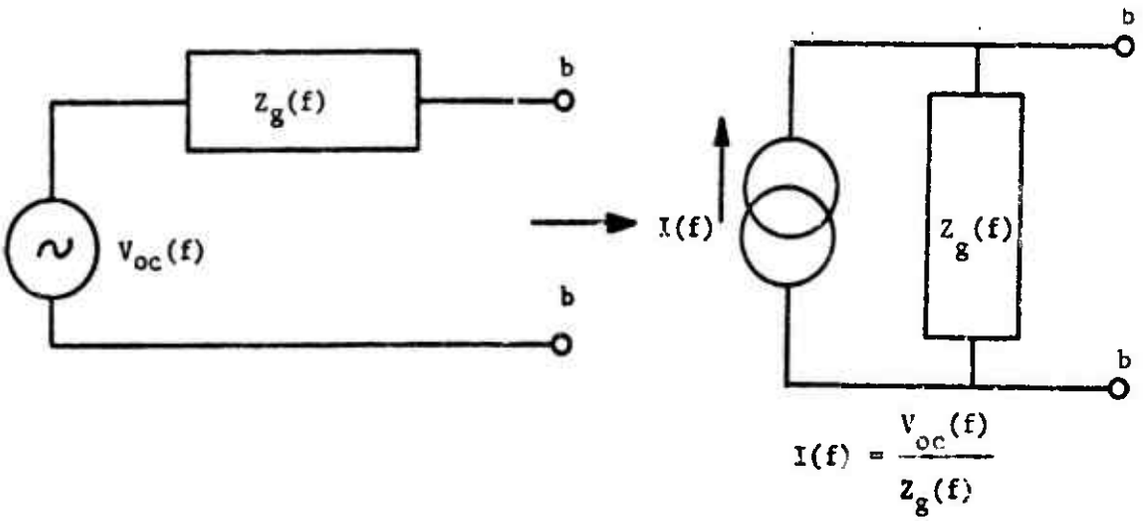


Figure E-2. Driving Source Equivalent Circuits

As it has been described above, single wire or single port Thevenin or Norton equivalent circuits can be determined for n-port networks. Although in actuality, a k port equivalent ($k \leq n$) can be constructed for any linear excitation and coupling network. The other n-k ports are terminated in their (linear) assigned values. Figure E-3 shows an excited coupling network (for example an illuminated cable).

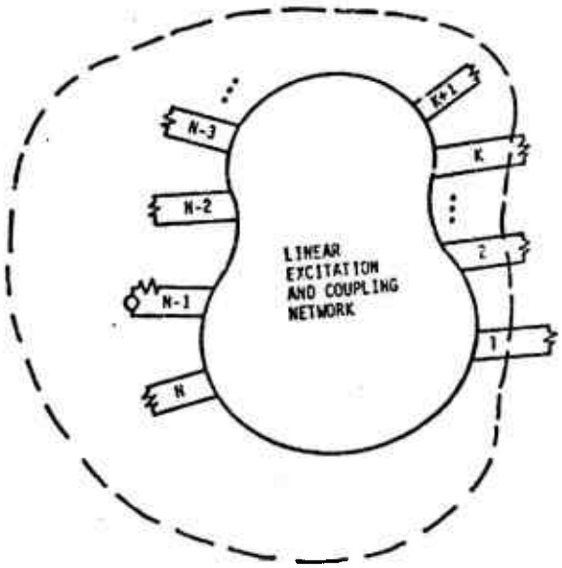


Figure E-3. An Arbitrary Coupling and Excitation Network

A k port Thevenin or Norton equivalent circuit can be defined within the dotted line. All ports within the dotted line are left connected to the appropriate terminations and the response of the network at any of the k ports can be determined for arbitrary (linear or nonlinear) terminations. Note that a common reference can be assigned for each of the k ports and so equivalent circuits of an excited cable can be found. When an equivalence of a linear active system is determined at a pair of terminals, it is accomplished by an application of Thevenin's theorem which states that a linear network with sources may always be represented by a voltage source equal to the open circuit voltage of the network in series with the network with all of its independent sources removed. This is depicted in Figure E-4.

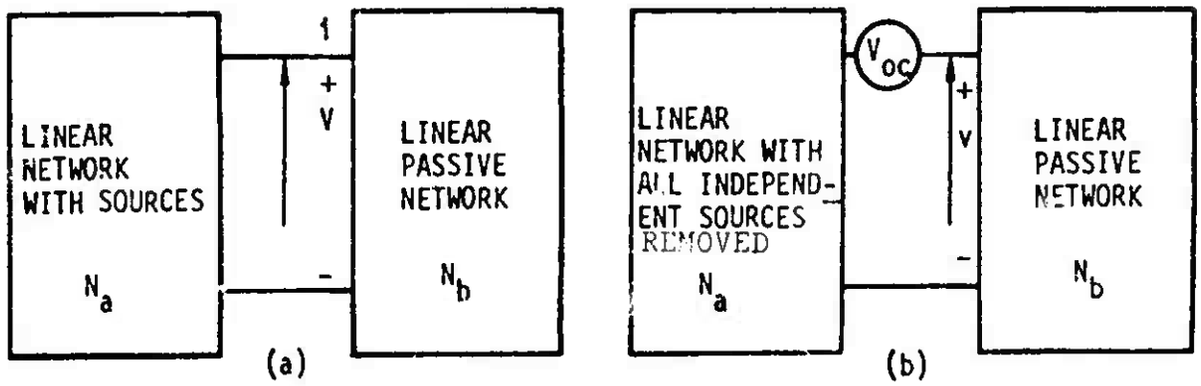


Figure E-4. (a) Original Network; (b) Thevenin Equivalent Circuit

For an n terminal (plus a ground terminal) network the system may be diagrammed as shown in Figure E-5.

If the network N_b is removed, $C(n + 1,2) = (n + 1)!/(2!\ (n - 1)!) = n(n + 1)/2$ open circuit voltages may be measured on the network N_a. However, $C(n - 1,2)$ of these voltages involve differences on the other n voltages and are thus dependent. For convenience the n node-to-ground circuit voltages are chosen as the independent set.

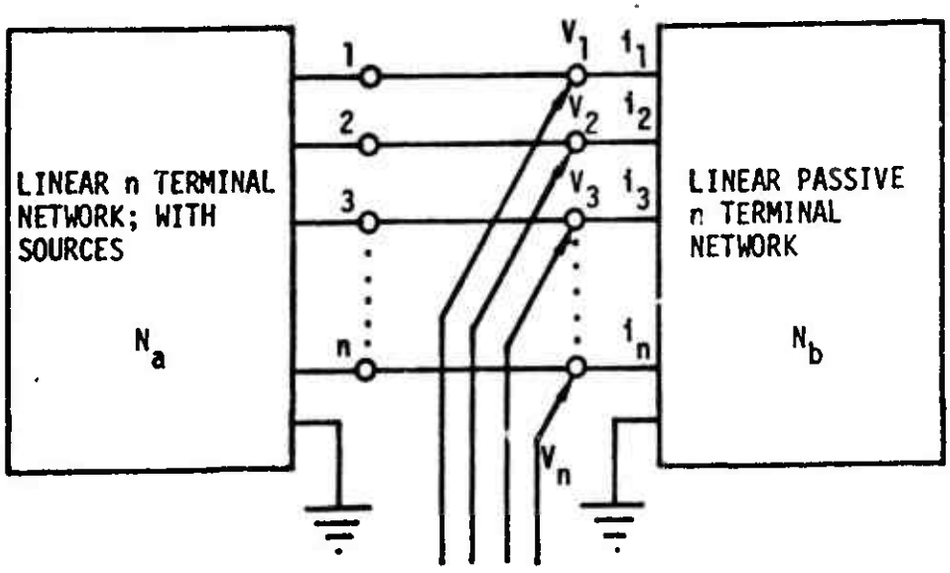


Figure E-5. N Terminal Networks N_a with Sources; N_b Passive

With all of the independent voltage sources removed from N_a, the remaining network can be represented by an n x n nodal admittance matrix. The value of the matrix elements can be determined by applying a 1-volt source between the appropriate terminals while simultaneously shorting the uninvolved terminals. The resulting current is the value of the appropriate admittance entry. Refer to this matrix as Y_a. The nodal admittance matrix for N_b will be referred to as Y_b. Assume that the two sets of measurements indicated have been made.

Now, return the sources to the network N_a. Apply voltages $-v_j^\circ$ to the terminals of N_a and the net voltage at each terminal will be zero. If the network N_b is again attached, no currents will flow between N_a and N_b. If the actual source generators are again turned off, the response is as if the set $(-v_j^\circ)$ were acting on terminations $Z_a = Y_a^{-1}$ and $Z_b = Y_b^{-1}$ connected in series. The responae to the actual source voltages acting alone is just the negative of this response. Thus the network can be represented as in Figure E-6.

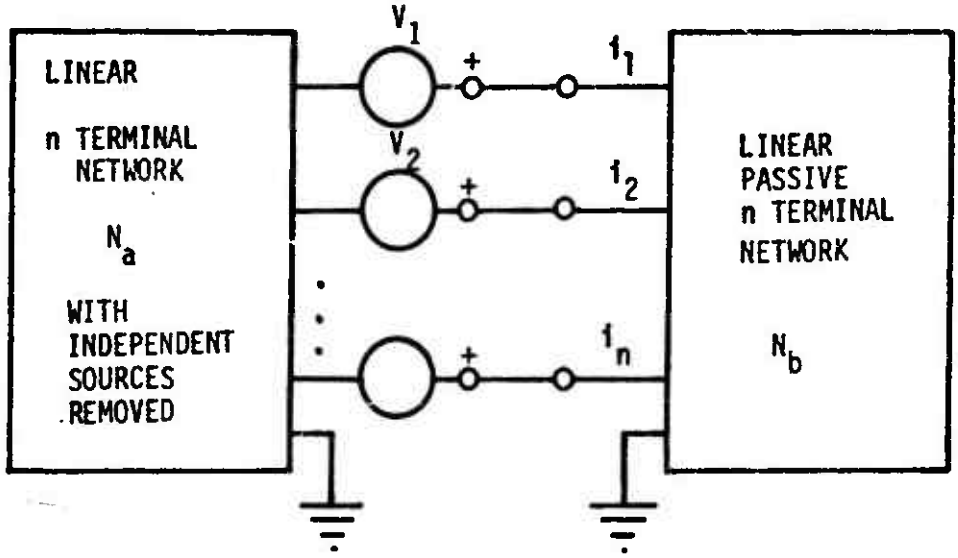


Figure E-6. A Generalized n Terminal Thevenin Equivalent Circuit

This general k port Thevenin Equivalent (or Norton Equivalent if desired) becomes a means whereby a large section of the total cable system problem can be reduced to only those variables directly applicable to further analysis or assessment. Integrating this technique with other analysis techniques such as the common mode current approach will yield estimates of responses at connector pins to subsystems that will allow assessment of EMP damage and upset.

2. EXAMPLES

A number of different types of equivalent circuits will be shown here representing cable source characteristics of several different cable configurations and EMP sources. All examples will be associated with the shielded cables shown in Figures E-7 and E-8. The EMP excitation of the cable based on the B-1 common mode current will be specified by the particular examples below and will consist of one of the circuits described

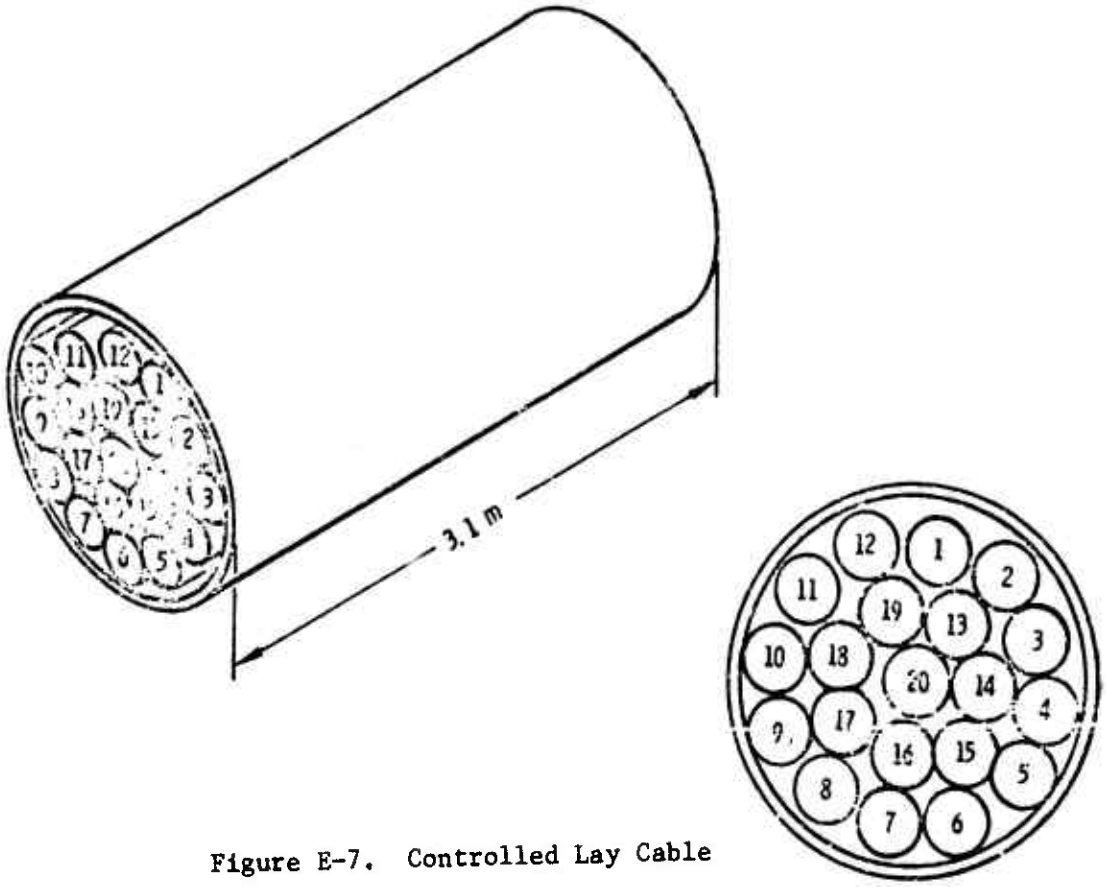


Figure E-7. Controlled Lay Cable

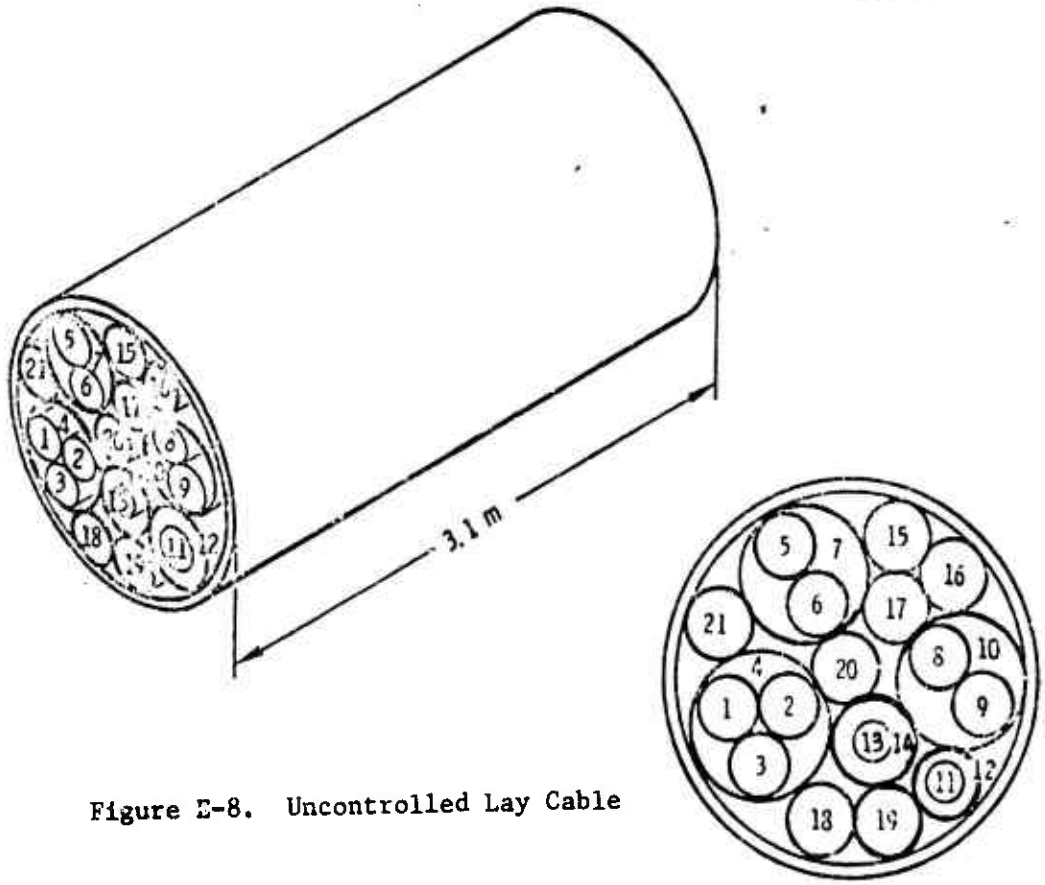


Figure E-8. Uncontrolled Lay Cable

in Figures E-9 through E-11. The load terminations for the cables shown in Figures E-9 through E-11 range from 1 ohm to 10 K ohms in a random fashion. The source terminations for the cable in Figure E-10 are identical to the load terminations described above. The equivalent circuit examples below will be categorized as one-port Thevenin or Norton Equivalent k-port Norton Equivalent and k-port Admittance Network for future reference.

a. One Port Thevenin or Norton Equivalent

(1) Norton Equivalent

Considered here is the controlled lay cable of Figure E-7 terminated and driven as shown in Figure E-9. A one-port Norton equivalent is shown in Figure E-12 where $Y_n = \frac{.18}{S + .12}$ and $I_{sc} \leq 3A$ peak for a 1 MHz damped sine wave (See Figure E-9).

The admittance Y_n has been synthesized to show the equivalent circuit in terms of circuit elements. The operator S in the admittance expression represents the scaled complex frequency independent variable and is equal to $\frac{j\omega}{2\pi \times 10^6} = jf$ where f is frequency in MHz and ω is the radian frequency in radians/second.

(2) Thevenin Equivalent

This example is a one port Thevenin equivalent for the uncontrolled lay cable shown in Figure E-8. The cable is terminated and driven as shown in Figure E-9 except for the internal shields which are shorted to ground at the load end. The Thevenin circuit is shown in Figure E-13 where $Z_{th} = .53(St.1)$ and $V_{oc} \leq 10$ V peak.

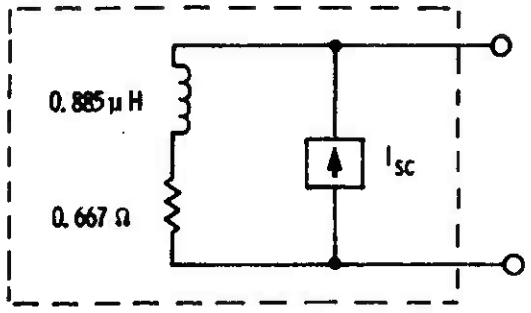


Figure E-12. Norton Equivalent Circuit

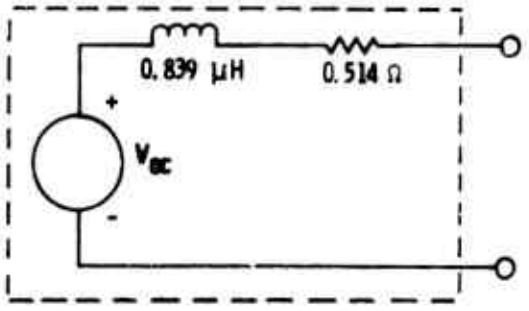


Figure E-13. Thevenin Equivalent Circuit

(3) Internal Shields Left Open at Load End

This csse is identical to case (2) with the exception thst the internal shields are left open at the load end. The Thevenin circuit is shown in Figure E-14 where $Z_{th} = .83(S + .1)$ and $V_{oc} \leq 15$ V peak.

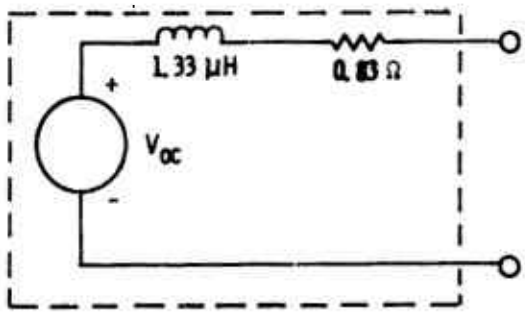


Figure E-14. Thevenin Equivalent Circuit

(4) Controlled Lay Cable

The cable considered here is the controlled lay cable shown in Figure E-7 and terminated as shown in Figure E-10. Two equivalent circuits were generated for this cable corresponding to two different source impedance values. For this case wire number 1 is selected representing a conductor with a 100 ohm source impedsnce. The equivalent circuit is shown in Figure E-15 where

$$Y_n = \frac{.58\ (S + 2.3)}{(S + 4.7)^2 + 16^2}$$

and $I_{sc} \leq 1$ mA peak resulting from the shield drive.

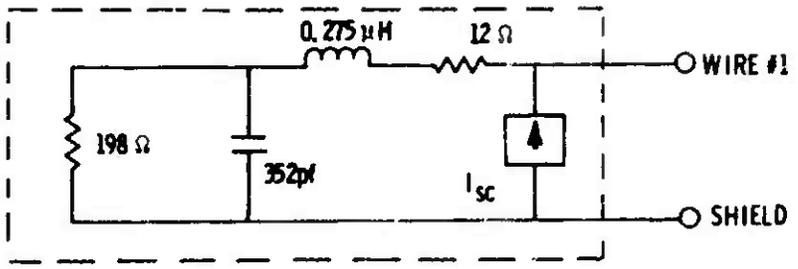


Figure E-15. Norton Equivalent Circuit

(5) Wire Number 15 Model

The equivalent circuit that is shown in Figure E-16 represents the same cable configuration as in (4) except for the conductor chosen for modeling. This model is for wire number 15 which has a one ohm source termination. Here $V_{oc} \leq .1V_{pk}$ and $Z_{th} = .77(S + .17)$.

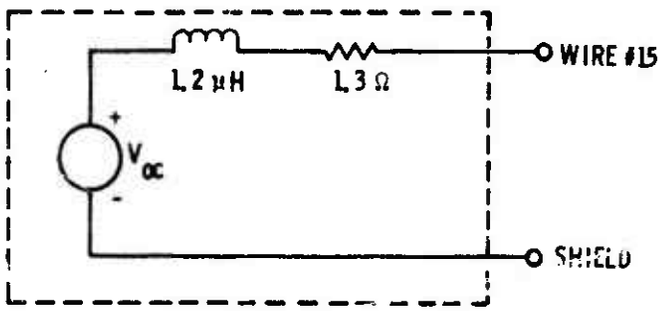


Figure E-16. Thevenin Equivalent Circuit

All the single wire equivalent circuits shown in examples (1) through (3) represent any wire chosen in the cable accurately. But example circuits (4) and (5) are quite different. The first statement is true because all the conductors at the source were tied together and the cable was short. Any particular wire chosen would see nearly the same impedance looking towards the source. The second statement now becomes evident by noticing the wire modeled in (4) has a 100 ohm source termination and the wire modeled in (5) has a 1 ohm termination.

(6) Lay Cable 6.2 Meters Long

The cables from which single port equivalents were generated above portrayed relatively simple impedance characteristics. For this example the same controlled lay cable as described in Figure E-7 but twice as long (6.2 meters) was considered. The EMP source and cable termination configuration is shown in Figure E-9. The Thevenin equivalent is shown in Figure E-17 where

V_{oc} 8 V peak and

$$Z_{th} = \frac{(S + .1)\left[(S + .9)^2 + 16^2\right]}{.35\left[(S + .46)^2 + 8.6^2\right]}$$

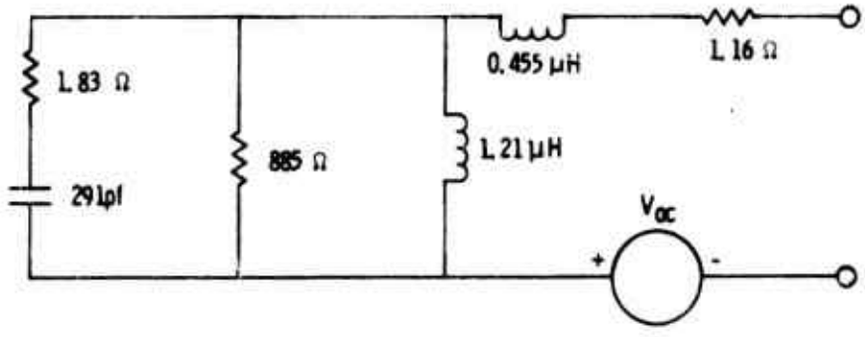


Figure E-17. Thevenin Equivalent Circuit

(7) Controlled-Lay-Cable-Generated Equivalent Single Port Circuit

The equivalent single port circuit shown in Figure E-18 has been generated from the controlled lay cable shown in Figure E-7. A set of 100 ohm resistors was used to connect the source terminations to the common mode current source as shown in Figure E-11. The load terminations are identical to the previous examples. The circuit elements were synthesized

from $$Z_{th} = \frac{(S + 3.2)^2 + 15^2}{.46\ (S + 1.6)}$$

and V_{oc} 10 V peak.

b. K-Port Norton Equivalent

A 3 port Norton Equivalent (Figure E-19) has been generated for the controlled lay cable shown in Figure E-7. The EMP source and terminations are defined by Figure E-9.

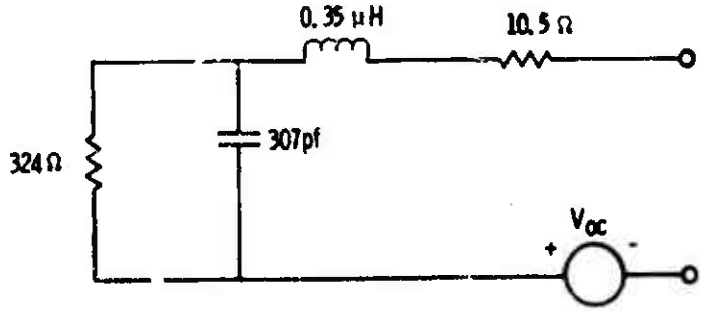


Figure E-18. Thevenin Equivalent Circuit

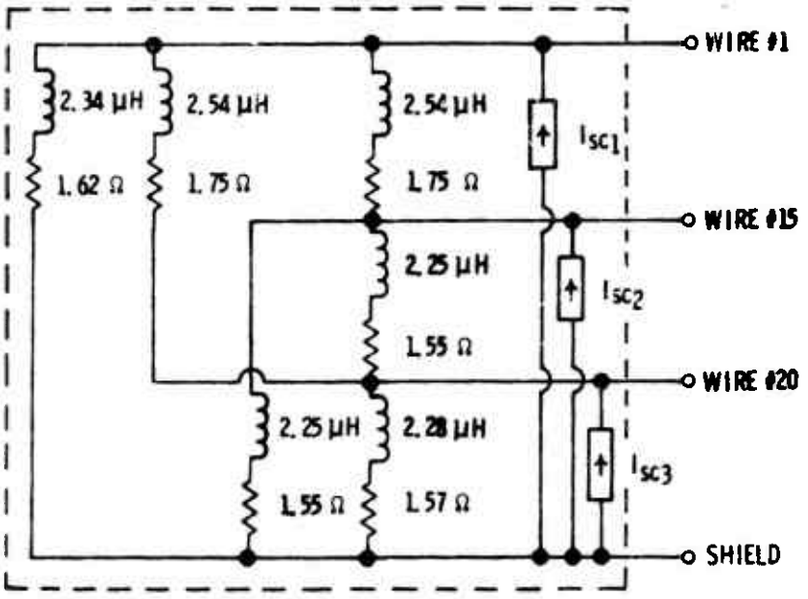


Figure E-19. Norton Equivalent Circuit

The Norton admittance in this case is depicted in matrix form as

$$\left[Y_n\right] = \begin{bmatrix} \frac{.194}{S + .11} & - \frac{.063}{S + .11} & - \frac{.063}{S + .11} \\ - \frac{.063}{S + .11} & \frac{.194}{S + .11} & - \frac{.071}{S + .11} \\ - \frac{.063}{S + .11} & - \frac{.071}{S + .11} & \frac{.205}{S + .11} \end{bmatrix}$$

and the Norton current (I_{sc}) is defined in Vector form as

$$\left[I_{sc}\right] \leqq \begin{bmatrix} 3 \\ 1 \\ .6 \end{bmatrix} \text{ Amps Peak}$$

c. K-Port Admittance Network

A 2-port network with an input port and an output port is shown in Figure E-20. The output port corresponds to a particular wire. The input port corresponds to the source of the cable where the common mode current source would be connected. Considering this as the controlled lay cable (Figure E-7) the model represents the passive cable configuration depicted in Figure E-9 with the current source (I_{B-1}) and source impedance (R_{SH}) removed.

Now

$$\begin{bmatrix} I_{in} \\ I_{out} \end{bmatrix} = \begin{bmatrix} \frac{.54}{S + .1} & - \frac{.22}{S + .1} \\ -\frac{.22}{S + .1} & \frac{.23}{S + .1} \end{bmatrix} \begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix}$$

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13. ABSTRACT

The goal of this handbook for EMP Electronic Analysis is to provide the circuit designer with techniques and models for use in assessing the degree of hardness of the circuits he is designing. New concepts and interpretation of existing techniques are presented and serve as a basis for defining the future effort required to provide a complete subsystem analysis capability. Topics covered are:

1) A brief overview of the various facets of a susceptibility threshold analysis.

2) A discussion of upset threshold analysis including response considerations, selection of analysis method, data, and examples.

3) An analysis of the problem of circuit damage thresholds encompassing the same areas as 2).

4) A description and illustration of methods for determining cable source characteristics.

Also included are several appendicies which present some analysis details, a semiconductor damage data base and a discussion of the Driving Point Impedance (DPI) analysis method.

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Security Classification

14. KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
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Circuit Analysis						
Subsystem Susceptibility Analysis						
Circuit Upset						
Circuit Damage						
Cable Source Characteristics						
Semiconductor Damage Data						
Driving Point Impedance (DPI)						
Circuit Analysis Method						